TABLE 10.9-1.
Semiconductors, M9.

1.	U1	80C39 Microprocessor	CPU
2.	U2	74HCT573 Octal latch	Lower Address Byte Latch
3.	U3	2716 2 k x 8 ROM	Program Memory
4.	U4	6116 2 k x 8 RAM	System Memory
5.	U5-U9	4094 8-bit Shift Registers	Transceiver Control
6.	U10	4104 Level Shifter	Buffering
7.	U12	4060 Oscillator/ Divider	Low-speed Timing
8.	U14, U15	78L08, LM340-5 Regulators	On-board Supplies
9.	U16	14528 Dual One-shot	SC Timer & INT Pulse
10.	Y2	3.2V Lithium Cell	Memory Retention

finishes doing what it has to do and shuts itself down again (this is called a "sleep").

10.9.2.2 OPERATIONAL DESCRIPTION

Upon power up, the reset capacitor C2 is charged from the zero-voltage state; and when the internal threshold is reached, the processor starts executing intructions. The sequence is for the CPU to first fetch the instruction from the program memory, U3, by asserting a low level on the PSEN line. This enables the ROM to write data to the data bus and the CPU can then read the data. Just before this operation the CPU has made sure that the address has been latched by U2 by exercising the ALE line which pulses high.

The processor then executes the instruction while preparing to fetch the next one. Some instructions will involve the access of the system storage memory, U4. This access is similar to the ROM access of above, but the RAM may, of course, be written to as well as read; so the direction of the data flow on the bus is determined by the assertion of one of the two direction lines, "RD" or "WR." These signals pulse to a low logic level when the access is made. "WR" is tied directly to the "WR" line of the RAM, and the "RD" line is tied to the output enable line (OE). Please refer to the INTEL or OKI data books for a complete description of all machine states. It is beyond the scope of this manual to provide detailed descriptions of the workings of the CPU and its place within the generalized system architecture.

10.9.2.3 MEMORY ENABLE SWITCH

A transistor, Q1, is used to change the state of the chip enable (CE) line of the RAM when powering up or down. When the set is turned on, the transistor conducts and assures a ground on the CE line, to enable the OE line to control the outputs. When the set is switched off, the transistor no longer conducts, shutting off at about +3 V. The switching threshold is set such that the CE makes its transition before power-down, and after power-up, but before the reset.

10.9.2.4 POWER-DOWN OPERATION

When the CPU is not being required to do anything, it detects this condition and shuts itself off. It then lies in wait for some activity. When the CPU is off, the crystal oscillator is shut down, all dynamic activity related to the CPU ceases, and the I/O lines are latched. In this "sleep" state, transceiver performance cannot be compromised by noise from the CPU and its associated circuitry since no signals are changing state.

There are several signals wired into the M9 module which are capable of waking up the CPU, which will then poll the lines to see which one caused the service request (SRQ). All these lines are connected via isolating diodes to the INT line of the CPU, and they all go to ground (0 Vdc) when requesting service. The CPU will remain awake as long as the INT line is low. When the SRQ signal is removed, the CPU will perform any remaining "housekeeping" functions and shut itself off again.

It takes the CPU a finite amount of time to wake up and shut down. This time is dependent on several factors, including the crystal activity and parasitic capacitance of the oscillator circuit as well as internal differences within the CPU itself. The SS signal, pin 5 of the CPU, is used to restrain the CPU from beginning execution until all the above listed parameters have stabilized. This is done by putting a shunt capacitance at the pin. There is an internal pull-up resistor which forms a time constant for start-up. The shut-down portion is not as critical.

The 0.1-microfarad capacitor provides roughly a 10-ms time constant. The routine "housekeeping" functions do not ever take more than about 5 ms, so that the CPU has plenty of time to do its tasks; in reality, it spends the great majority of its available processing time waiting in loops or asleep.

10.9.2.5 SERVICE REQUESTS

There are four sources of SRQ's in the system. They are:

1. PTT operation.
2. Key depression.
3. Selective call alarm.
4. Scan mode enabled.

These signals and their causes and effects are discussed in the paragraphs that follow.

As stated, the normal state of the CPU is inactive, that is, asleep. When an SRQ is detected, the CPU begins polling the various possible sources until it finds the one which was the cause. There is an order of priority given to the four sources.

The PTT operation is checked first for fast response. If the INT line is being held down by the conduction of Q3, then P13 of the CPU will also be low through D6 and the CPU reads this line to see if PTT has been pressed. If this is the case, the CPU then fetches the programmed transmit frequency information from the system memory, retunes the synthesizers and reselects the proper harmonic filter, if necessary. It has then done its job and waits for the PTT to be released. It then reloads the programmed receiver frequency and retunes the transceiver.

Before shutting itself down each time, the CPU sets the column lines of port 1 to all lows. In this way, when one of the sixteen possible keys is pressed during the sleep state, a low will be forced on the INT line through one of the diodes D2-D5. The CPU will then wake up and read the four row lines to see if any of them is low. If so, the normal keypad scanning routine is executed and the key identified. This keypad scanning routine is described in the next subsection.

If the above two sources are not the cause of the SRQ, the CPU makes another test of the the INT line to see that it is still low. This double-check is useful in eliminating the effects of any transients induced in the system. If INT is still low at this point, the program checks to see if P12 is also low. If this is the case, the CPU will recognize a selective-calling alarm condition, and the "CALL:" display is shown on the LCD, followed by the current channel number. If the INT is still low and one of the above sources cannot be identified, the program assumes it is a spurious response or a system failure of some kind and ignores it.

10.9.2.5.1 SCAN SRQ

The previously mentioned three sources of SRQ can cause the system to wake up whenever it is asleep. The final source of SRQ occurs only when using the scanning feature of the transceiver. As the scan button is pushed, the transceiver is tuned to the frequency stored in channel ninety (90) and the "SCAN:90" display is shown. Then the P26 line from the CPU is made high to enable a 1-Hz square wave from U12-15 to be fed into the trigger input of the "one-shot," U16. The square wave will trigger the "one-shot" on its falling edge. The output of U16-7 is a very short low-going pulse of 100 μs. This pulse is able to cause an SRQ through its diode and thus wake up the CPU to let it know it is time to go on to the next channel in the scan. This pulse occurs roughly every second, and has no effect on the recognition of the other SRQ sources. If the system is not being used with the selective-calling module, a second capacitor may be installed at U12 to yield a three-second scan.

10.9.2.6 LOW-FREQUENCY TIMING

U12 is a low-frequency oscillator and divider. Its oscillator runs at a frequency determined by the R/C network of U12, pins 9, 10, 11. Roughly 1000 Hz is correct for the one-second scan, and 330 Hz for the three-second scan. The divide-by-1024 output is used for the scan SRQ, and the divide-by-16 output drives the LCD backplane of M11. This yields a backplane frequency of from 20 to 60 Hz. The capacitors should only be replaced with mylar or polycarbonate types or other relatively temperature-stable constructions.

10.9.2.7 KEYPAD SCANNING

The keyboard is scanned by the CPU by setting all four column lines to the high state except one, which it makes a low. This tells what column is being scanned at any moment. If any of the keys in that column is pressed, the corresponding row line will also be pulled low. In this way the CPU can tell which button has been pressed.

If no key has been pressed in that column, the other columns are polled in order. If none of the keys is being pressed, the CPU will return from the polling routine and execute the sleep instruction and shut off. The entire poll takes much less than a millisecond, so the pulses seen on the column lines are short. If a key is being pressed, columns with numbers higher than the column containing the key being pressed will not be scanned.

10.9.2.8 INTERNAL SERIAL INTERFACES

As stated above, the four lines P24-P27 form two serial output ports that control the transceiver interface and the display interface. The operation of the two ports is similar in that each is composed of a clock line and a data line which together control the flow of serial data to the interface. The transceiver interface is slightly different in that "shift-and-store" type registers are used and a latch line is employed. The display interface employs simpler serial-in, parallel-out shift registers, as explained in the M11 section.

The display interface is inherently different in this respect because if the display were to flicker slightly as the data goes in, the eye would not be able to detect it.

Both interfaces shift the data in basically the same manner. The next data bit is presented on the data line, which is common to both interfaces. This line is U5-2 in the transceiver interface. Then the clock is toggled from zero to one to zero again, shifting the data in. Forty bits, or five bytes, of information are shifted into the transceiver interface every time it is updated. All the data are shifted in each time, and when clocking is complete, the latch line of the shift registers, pin 1 on U5 through U9, is toggled from zero to one to zero again, allowing the shifted data to be presented at the outputs, pins 4-11 on U5 through U9.

The display interface requires 64 bits to be shifted in each time it is updated. In the above case of the transceiver interface, it is easy to identify each bit of the output with its position in the serial data stream. The display drivers

are arranged such that each bit drives a segment of the LCD. The order is independent of the natural order of the segments and can be determined by looking at the schematic diagram of the M11 module. Usually this is not important for troubleshooting anyway, since if any data is coming out at all it is almost sure to be right.

10.9.2.9 SELECTIVE CALLING MODULE INTERFACE

The other half of U16, the "one-shot" chip, is used in conjunction only with the selective-calling module (SCM) and serves as the preamble timer. There are four control lines brought from the SCM which are used to control the length of the preamble and sense the state of the SCM's receiver.

The S.C. initiate line is diode isolated and connected to U16-11. This is the falling-edge trigger input of the timer. When the SCM "SEND" button is pressed, this line goes low, firing the timer. The timer's "not-Q" output is returned to the SCM, where it holds the preamble on and keeps the code from being sent until the timer times out. When this output at U16-9 returns high, the SCM code is transmitted and the call terminated. The timer period is fixed at roughly 12 seconds ±1 second. This period gives all the scanning receivers in the net enough time to cross the calling frequency when all 10 channels are being used.

The two other lines are used to detect the presence of a received SCM valid preamble, and the SCM alarm when it occurs. P23 of the CPU is dedicated to inputting the preamble detect signal, which is normally at a low level. When the preamble is heard on frequency, this line goes high. When the transceiver is in the scanning mode, assertion of this signal causes the scan to halt. It will remain halted until the signal is low again. There is a delay of about 8 seconds before scanning is resumed to avoid losing the call because of the effects of selective fading, noise, etc.

When the alarm line which is tied through diodes to CPU lines as described above goes low, the scan is stopped for about 60 seconds and the "CALL" display called up. The scan will resume but the "CALL" display will remain. Reception of one call does not stop the reception of another call. The scan may be stopped manually to cancel the "CALL" display. The "CALL" display will also appear on any channel when the correct SCM call is received. In this case, press any button to cancel the display.

10.9.2.10 LCD BACKLIGHT SUPPLY

U11 is an encapsulated circuit which is responsible for powering the LCD backlight. It takes +12 V switched through the "LIGHT" switch as its supply, and puts out the several-hundred-Vac waveform to power the backlight. The output shape of the ac signal is not particularly critical, as long as at least 100 Vac RMS is present.

10.9.2.11 DC REGULATORS

The standard three-pin regulators are used to provide the dc power for the circuits. The 8-V regulator is adjusted up to 8.7 V by D13. This is so that the interface outputs can drive CMOS IC's which are running off +12 V if necessary.

10.9.2.12 AUDIO MUTING

Q2 is a transistor which is made to conduct whenever the CPU is running. Its collector is routed into the M1 module, where it is able to shut off the squelch gate FET when on. When the CPU goes to sleep, the transistor is shut off and the audio resumes.

10.9.3 TEST PROCEDURE

NOTE

The following signal checks must be made with one of the buttons depressed to start the system clock. Conditions in the absence of the key depression will be static.

10.9.3.1

While a button is being pressed, check for the "ALE" signal at U1-11. It is a positive-going pulse with a period of about 2.9 microseconds.

10.9.3.2

Check for a PSEN signal, a negative-going pulse with roughly the same 2.9 microsecond period, at U1-9.

10.9.3.3

Check for the presence of the WRITE signal, a negative-going pulse of microsecond duration which occurs when the channel, frequency, or other parameters are changed. Enter CH 00. Begin to change the frequency and observe the pulse at U1-10.

10.9.3.4

Look at U9-3 while the "F" button is being pushed over and over again. There should be a train of 64 positive-going pulses either when the button is pushed or released. The time required for the pulse train will be a millisecond or two.

10.9.3.5

Look at U9-2 while again pressing and releasing the "F" button. A serial data stream corresponding to the clock periods of step 4 above should be seen. Clock and data at this point are 8-V levels.

10.9.3.6

Look at U9-1 while again pressing and releasing the "F" button. The signal should be low during the data stream and high (+8 V) afterwards. When the button is released, the level should go low again.

10.9.3.7

Check U1-37 for another clock data stream which updates the display interface after a key depression.

TABLE 10.9-2.
Internal Connections.

J4 Connector Pin	Line Description
4	KEY--keys the transmitter on for low-level carrier tuning. An open-collector NPN transistor capable of sinking 0.5 A to ground when activated.
2	+12 Vdc--Nominal 12 V at 1.5 A, maximum.
1	Ground.
5	Initiate Tune--Starts tune cycle. Normally open line; tune at pulse is a momentary closure to ground.

10.9.3.8
Look at U12-15 for 5-V, 1-Hz square wave. Look at U16-5 while in the SCAN mode. The 1-Hz square wave should be present. Stop the scan, and the square wave should disappear.

10.9.3.9
Press the "DOWN ARROW" button and hold it down. Observe the column-scanning pulses at U1-27 through 29. The pulse width should be negative-going, about 5 microseconds. The pulse width on U1-30 should be much greater, but the period of repetition should be the same as the others.

10.9.3.10
Verify that each of the lines U1-31 through 34 goes low as a button in its respective row is pushed.

10.9.3.11
Verify that the INT line of U1-6 goes low when either a button is pressed, the S.C. alarm line is pulled low, the T+ line is raised, or the SCAN mode is enabled. In the case of the SCAN mode, check for a 100-microsecond pulse at one second intervals.

10.9.3.12
Check U12-7 for the presence of a square wave with roughly a 20-millisecond period. This signal powers the LCD backplane.

10.9.3.13
Verify that the signals at U1-1 and U1-39 toggle when their respective switches are flipped.

10.9.3.14
Monitor U4-18. Switch the power off and observe that the voltage being monitored goes high before the supply falls below the +3-V level. Observe that when the power is turned back on, the opposite occurs and the signal flips low before the supply reaches +5 V.

10.9.3.15
Verify that the voltage on U4-24 is greater than 2 V when the power is shut off. If the voltage is less than 2.5 V, the cell should be replaced. See Table 10.9-3.

10.9.4 TROUBLESHOOTING

10.9.4.1 TROUBLESHOOTING PROCEDURE
Table 10.9-3 describes the troubleshooting procedure for the M9 and M11 modules.

10.9.4.2 CELL REPLACEMENT Y2
To replace the Y2 lithium cell, remove the bottom cover of the unit. Gain access to the M9 module, and power the unit up. Carefully remove the cell by sliding it out sideways with a non-conductive tool. Slide in the new cell with the positive side up. Measure the cell voltage and current after the transceiver has been powered down again.

Current is typically less than 1 microampere at ambient temperatures, and will increase with increasing temperature; likewise, the current will decrease with decreasing temperature. Nominal fresh cell voltage is 3.2 V.

10.9.5 ANTENNA TUNER INTERFACE
The transceiver is designed to work with Transworld's RAT100 automatic antenna tuner without any modifications. The interface circuitry necessary to control the antenna tuner is contained on the M9MP circuit board. All tuner control lines are routed from this circuit board to the J4 rear panel connector.

The RAT100 is an automatic antenna tuner designed to operate with the transceiver to automatically match the 50-ohm output of the transceiver into a variety of antennas for mobile, marine and base station applications over the frequency range of 2-30 MHz. All operation, including network tuning and VSWR monitoring, is fully automatic and microprocessor controlled. Tuning time is typically two to three seconds.

Tuning is fully automatic. The tuner is connected to the transceiver by a 4-wire or 8-wire control cable (depending on whether the memory option is used). Supply voltage is

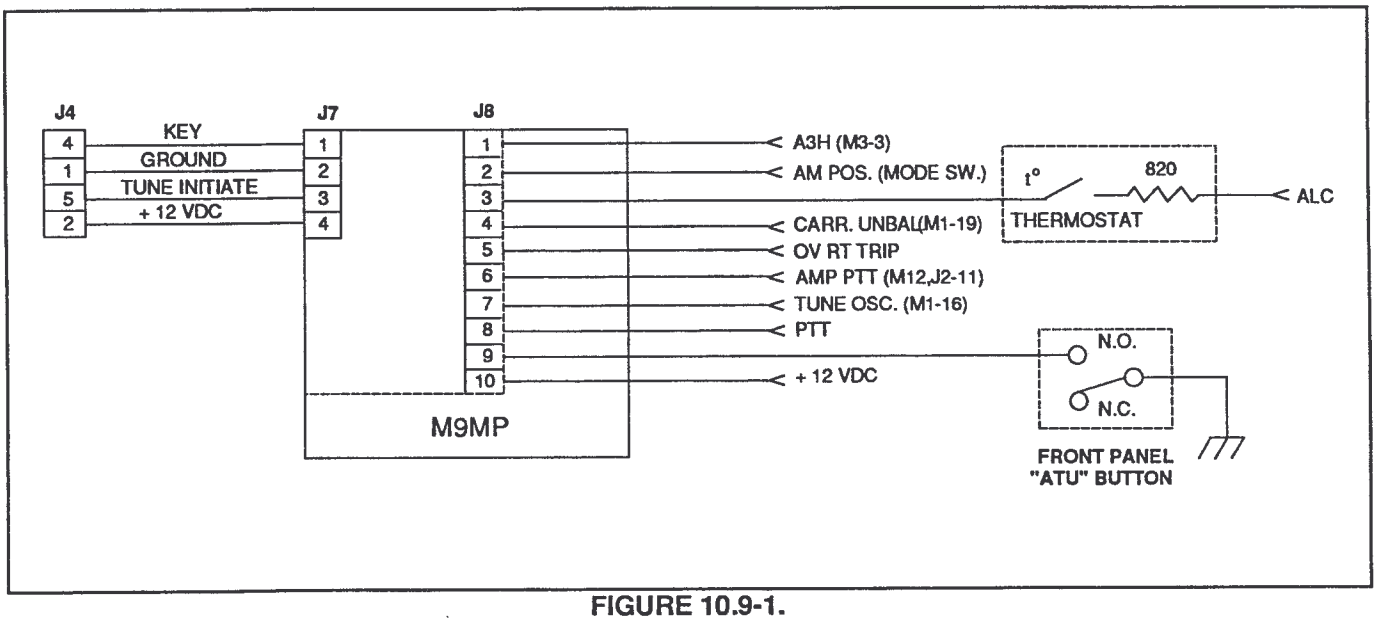


FIGURE 10.9-1.
Transceiver Wiring.

12 Vdc and is supplied by the transceiver. Upon receipt of a TUNE INITIATE pulse from the transceiver, the tuning elements are all switched to a HOME position. The tuner generates a KEY signal which enables both the transmitter carrier output and the low-power ALC. At this time, a signal is also provided which activates the TUNING tone in the transceiver. When RF tune power is received, the tuner automatically matches the antenna to a VSWR of 1.5:1 or less within 3 seconds (typically, 1 second).

When tuning is completed, the coupler releases the KEY signal and disables the tuning tone in the transceiver; normal transmissions from the transmitter are then allowed.

10.9.5.1 CONNECTIONS

The tuner control cable plugs into the transceiver J4 connector. Internal wire descriptions are defined in Table 10.9-2. The mating cable connector on the tuner end is a MS3106F-8-27S and is supplied with the tuner. Instructions for cable fabrication and hook-up are provided in the RAT100 technical manual.

The RF connection between the tuner and transceiver should be made with a good gauge of RG8/U-type 50-ohm coaxial cable. The tuner end of the cable should be terminated with a UG-21C Type-N connector, while the transceiver end is terminated with a male UHF connector.

10.9.5.2 OPERATION

After installing the antenna and the tuner, it is only necessary to connect the tuner to the transceiver using the multiwire control cable and RF coaxial cable described in Section 5.

10.9.5.3 OPERATION WITH TRANSCEIVER

The following procedure should be followed when operating the RAT100 with the transceiver.

NOTE

The carrier is automatically disabled from operating open-loop during the tune cycle if the mode switch is in the AM position.

a. Select the operating mode of the transceiver, i.e., LSB, USB, AM or REMOTE.

b. Turn on the power using the transceiver front-panel switch. Note that there are no operator controls on the tuner.

c. Select the transmitter operating frequency.

d. Press and then release the ATU button on the front panel.

After the ATU button is pressed, the tuning tone in the transceiver should come on, indicating that a tune cycle is in progress. During this period the tuner holds the transceiver key line down (transmit mode) until the tune cycle is completed. Upon completion of the tune cycle, the tuning tone goes off and the key line is released. The system is ready for use when the tuning tone goes off.

NOTE

The transceiver must be unkeyed when the ATU button is depressed in order to activate the tune cycle. The tuner will <u>not</u> start a tune cycle if transmit power is present <u>before</u> the button is pressed.

NOTE

If the transceiver is being operated using remote control, then antenna tuning is accomplished by pressing the "ATU" key on the remote control console (after operating mode and frequency have first been inputted).

10.9.5.4 THEORY

A complete description of the tuner is given in the RAT100 technical manual. Control of the various functions is accomplished by the circuitry on the M9MP board in the transceiver. A schematic of this circuit is shown in Figure 10.9-4, and a wiring diagram showing internal transceiver connections is given in Figure 10.9-1.

Operation is as follows: during normal transceiver receive and transmit periods transistor Q101 is biased ON by R101, D103 and R118. This means that the collector of Q107 is at zero (tone oscillator OFF), and Q102, Q103, Q106, and Q108 are OFF. Therefore, Q104 and Q105 are ON, thus activating the high-power ALC and connecting the A3H line (M3-3) to the AM position on the mode switch. When the ATU button on the transceiver front panel is depressed, a ground signal is sent to the tuner; upon receiving this ground pulse, the tuner grounds the key line (J7-1) and turns transistor Q101 OFF. This applies power to the tone oscillator Q107, which turns on and puts out a 1.5-kHz audio tone to the audio amplifier in the M1 module. Q106 is turned on, which grounds the transceiver PTT line and keys the transmitter; and Q108 turns on to unbalance the modulator in the M1 module, which allows the carrier to be transmitted. At the same time, Q104 is turned OFF, which activates the low-power ALC and limits the output to 10 W; and Q105 is turned OFF, which prevents the transceiver from operating in AM mode during the tune cycle. When the tuner has formed a satisfactory match, it releases the key line and conditions revert to normal. Q15 is a Darlington transistor which provides the PTT for an external amplifier. This PTT can be inhibited by the Remote Control when required, and is always inhibited during any antenna coupler cycle.

TABLE 10.9-3.
Troubleshooting Procedure.

STEP FAILED	R/R COMPONENT	CHECK RELATED SIGNALS
1.	U1	U1,2 ; U1,3 Xtal Oscillator U1,4 Reset U1,5 Single Step
2.	same as 1.	
3.	check as 1. above U2 U3	 All All
4.	U1 U10	U1,35 Clock Out U10,4 ; U10,3
5.	U5 U6 U7 U8 U10 U1	U5,2 ; U5,9 U6,2 ; U6,9 U7,2 ; U7,9 U8,2 ; U8,2 U10,5 ; U10,6 U1,38 Data Out
6.	U1 U10	U1,36 Strobe Out U10,10 ; U10,11
7.	U1	U1,37 DIS CLK
8.	U12 U1 U16	U12,9 ; U12,10 U1,38 U16,5
9.	U1 D2-D7 Q3	U1,27-34 ; U1,6 U1,6 T+
10.	As 9. above	

TABLE 10.9-3.
Troubleshooting Procedure. Continued.

STEP FAILED	R/R COMPONENT	CHECK RELATED SIGNALS
11.	As 9. above D13-14	U1,6
12.	As 8. above	
13.	U1 S1 (U17)	U1,1; U1,39
14.	D10 Q1 R11 D8-9 U4	D10 Cathode Q1 Base U4, 24 D9 Anode U4, 18; etc
15.	D8-9 Y2	All Voltage Output

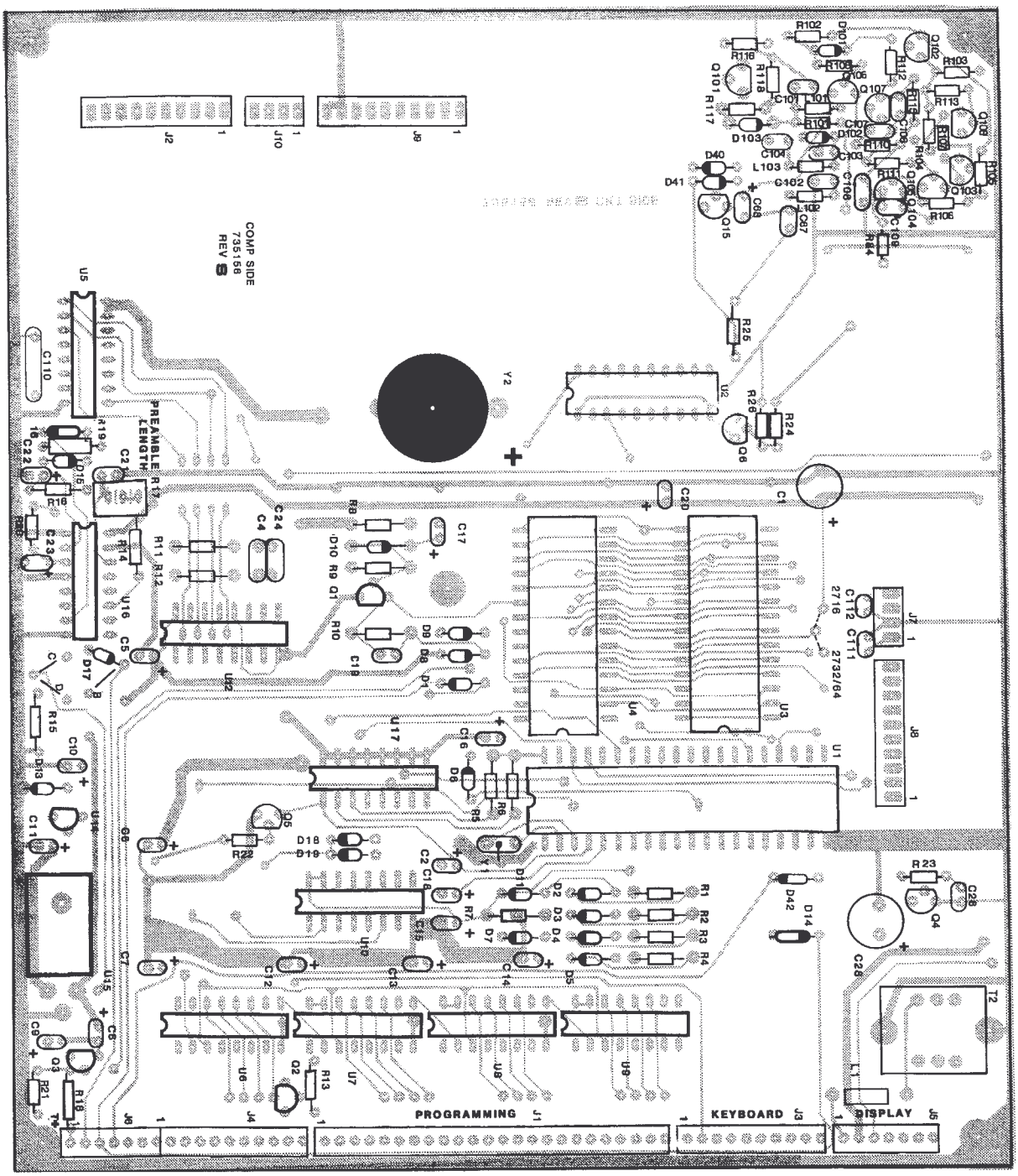
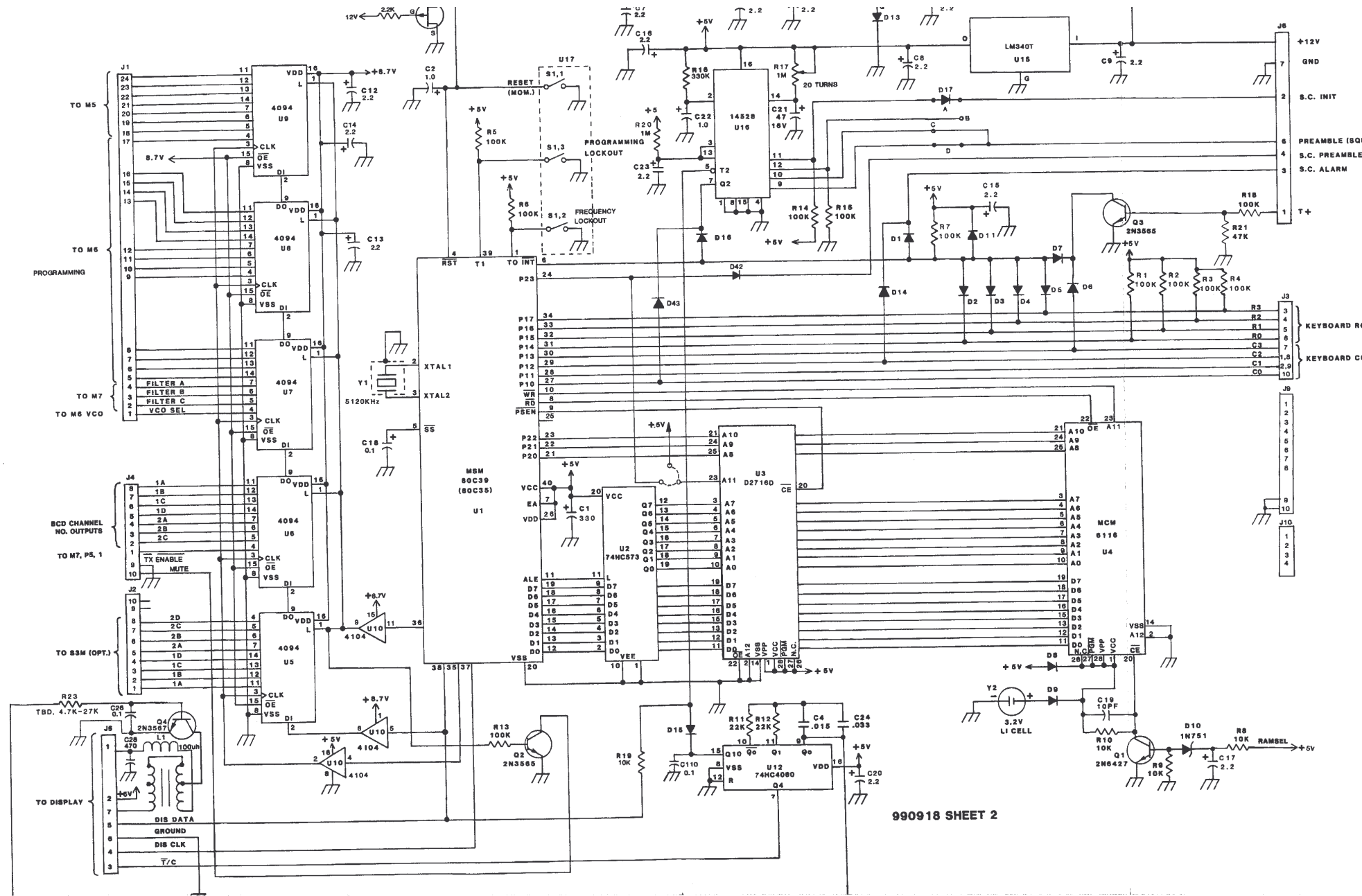


FIGURE 10.9-2.
Component Locations, Frequency Control Module.


990918 SHEET 2

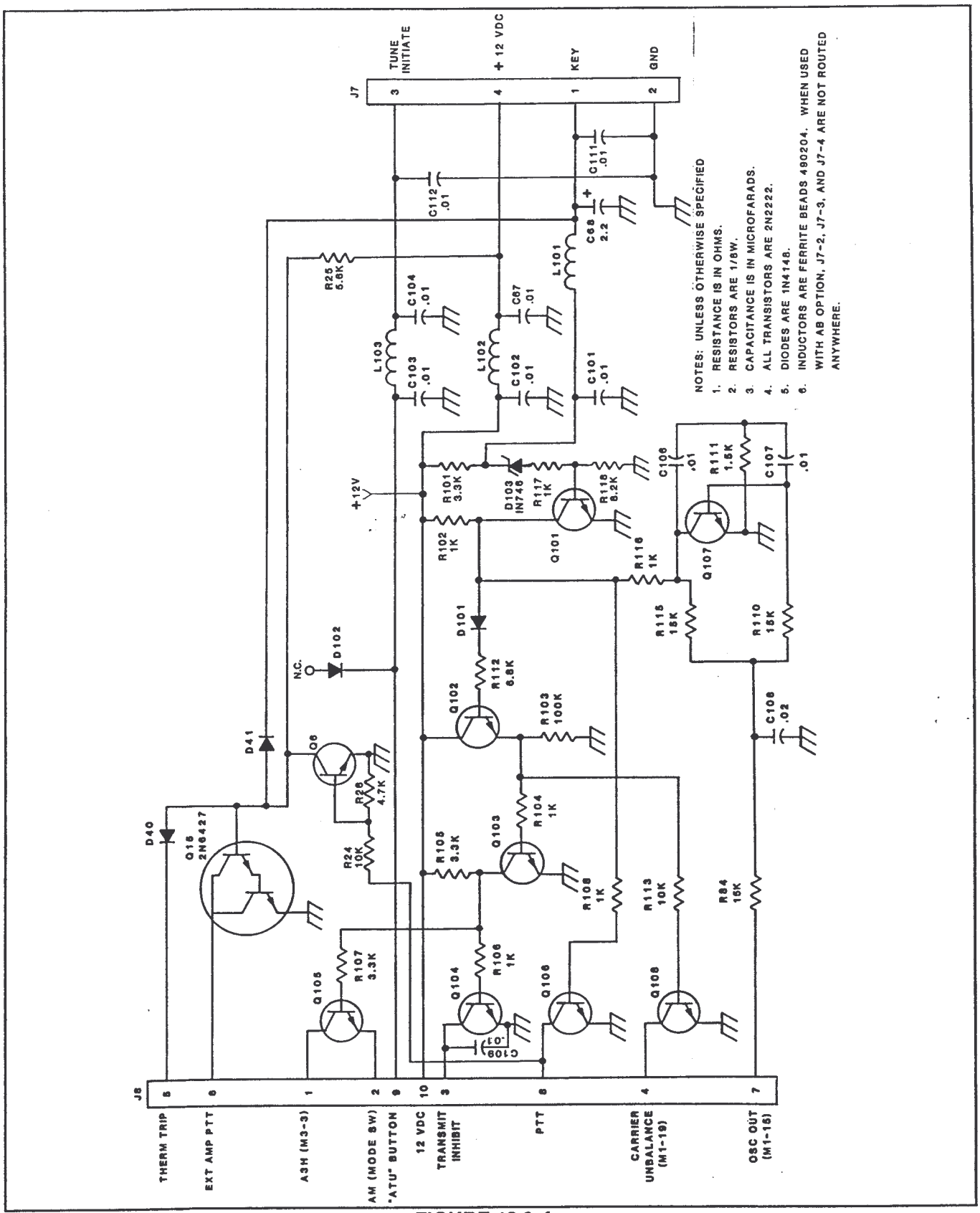


FIGURE 10.9-4.
Schematic Diagram, Antenna Tuner Interface.

TABLE 10.9-4.
Parts List, Microprocessor Module, M9MP.

C1	231331	Capacitor, Electrolytic 16 V 330 μF
C2	241010	Capacitor, Tantalum 1 μF
C3		Not Used.
C4	254153	Capacitor, Mylar 100 V 0.015 μF
C5-C17	241020	Capacitor, Tantalum 2.2 μF
C18	275104	Capacitor, Monolithic 50 V 0.1 μF
C19	210100	Capacitor, Disc NPO 10 pF
C20	241020	Capacitor, Tantalum 2.2 μF
C21	241476	Capacitor, Tantalum 47 μF
C22	241010	Capacitor, Tantalum 1 μF
C23	241020	Capacitor, Tantalum 2.2 μF
C24	254333	Capacitor, Mylar 100 V 0.033 μF
C25		Not Used.
C26	275104	Capacitor, Monolithic 50 V 0.1 μF
C27		Not Used.
C28	231471	Capacitor, Electrolytic 16 V 470 μF
C29-C66		Not Used.
C67	214103	Capacitor, Monolithic 50 V 0.01 μF
C68	241020	Capacitor, Tantalum 2.2 μF
C69-C100		Not Used.
C101*-C104*	214103	Capacitor, Monolithic 50 V 0.01 μF
C105*		Not Used.
C106*, C107*	214103	Capacitor, Monolithic 50 V 0.01 μF
C108*	254203	Capacitor, Mylar 0.02 μF
C109*	214103	Capactor, Monolithic 50 V 0.01 μF
C110	210104	Capacitor, Disc 25 V 0.1 μF
C111,C112	214103	Capacitor, Monolithic 50 V 0.01 μF
D1-D9	320002	Diode, 1N4148
D10	320204	Diode, Zener 1N751
D11	320002	Diode, 1N4148
D12		Not Used.
D13-D19	320002	Diode, 1N4148
D20-D39		Not Used.
D40-D43	320002	Diode, 1N4148
D44-D100		Not Used.
D101*, D102*	320002	Diode, 1N4148
D103*	320210	Diode, Zener 1N746
L1	430014	Inductor, Molded Min 100 μH
L101*-L103*	490204	Bead, Ferrite Shield
Q1	310064	Transistor, Darlington 2N6427
Q2, Q3	310006	Transistor, NPN 2N3565
Q4	310003	Transistor, NPN 2N3567
Q5	310072	Transistor, J175
Q6	310057	Transistor, NPN PN2222A
Q7-Q14		Not Used.
Q15	310064	Transistor, Darlington 2N6427
Q16-Q100		Not Used.
Q101*-Q108*	310057	Transistor, NPN PN2222A
R1-R7	113104	Resistor, Film 1/8 W 5% 100 kΩ
R8-R10	113103	Resistor, Film 1/8 W 5% 10 kΩ
R11, R12	113223	Resistor, Film 1/8 W 5% 22 kΩ

TABLE 10.9-4.
Parts List, Microprocessor Module, M9MP, Continued.

R13-R15	113104	Resistor, Film 1/8 W 5% 100 kΩ
R16	113334	Resistor, Film 1/8 W 5% 330 kΩ
R17	170213	Resistor, Trimmer 1 MΩ
R18	113104	Resistor, Film 1/8 W 5% 100 kΩ
R19	113562	Resistor, Film 1/8 W 5% 10 kΩ
R20	113105	Resistor, Film 1/8 W 5% 1 MΩ
R21	113473	Resistor, Film 1/8 W 5% 47 kΩ
R22	113222	Resistor, Film 1/8 W 5% 2.2 kΩ
R23	TBD	Resistor, Film 1/8 W 5% 4.7-27 kΩ
R24	113103	Resistor, Film 1/8 W 5% 10 kΩ
R25	113562	Resistor, Film 1/8 W 5% 5.6 kΩ
R26	113472	Resistor, Film 1/8 W 5% 4.7 kΩ
R27-R83		Not Used.
R84	113153	Resistor, Film 1/8 W 5% 15 kΩ
R85-R100		Not Used.
R101*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R102*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R103*	113104	Resistor, Film 1/8 W 5% 100 kΩ
R104*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R105*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R106*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R107*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R108*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R109*		Not Used.
R110*	113153	Resistor, Film 1/8 W 5% 15 kΩ
R111*	113152	Resistor, Film 1/8 W 5% 1.5 kΩ
R112*	113682	Resistor, Film 1/8 W 5% 6.8 kΩ
R113*	113562	Resistor, Film 1/8 W 5% 10 kΩ
R114*		Not Used.
R115*	113153	Resistor, Film 1/8 W 5% 15 kΩ
R116*, R117*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R118*	113822	Resistor, Film 1/8 W 5% 8.2 kΩ
T1		Not Used.
T2	410019	Transformer, 600/600 ohm line
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	Programmed, UPD2716D
U4	330149	IC, MCM6116P12 (120 ns)
U5-U9	330126	IC, CD4094BE
U10	330150	IC, F4104BPC
U11		Not Used.
U12	330240	IC, 74HC4060
U13		Not Used.
U14	330018	IC, 78L08
U15	330076	IC, LM340T-5.0
U16	330115	IC, MC14528BCP
U17**	530010	Switch, DIP SPST
Y1	360018	Crystal, 5,120.00 kHz
Y2	750015	Battery, Lithium Button

* Indicates part located on Automatic Antenna Tuner interface portion of PC Board.
**Mode Selection Switch - refer to Section 6.

10.10 RF POWER MODULE, M10

The M10 module is a two-stage, broadband, 1.6- to 30-MHz power amplifier module capable of putting out 150 W of RF power. It is located on the rear panel and mounted to the heatsink. The input comes from the M4 module and the high-power output goes to M7 for filtering, prior to going out to the antenna terminal.

10.10.1 TECHNICAL DESCRIPTION

10.10.1.1 MODULE INTERCONNECTIONS

Figure 10.10-1 is a component location diagram of M10, showing all PCB interconnections as well as component reference designations.

RF Connections

a) Transmit Input. Channel frequency signal from M4.
b) Transmit Output. High-power output at channel frequency to M7.

DC Connections (All connections made with spade lugs.)

a) +13.6 Vdc, Unregulated. Unregulated dc input from either ac power supply or dc input power. Provides voltage for second RF amplifer stage.
b) T+. Provides voltage for bias circuitry and first RF amplifier stage.
c) ALC Output. Output to ALC circuit from dc current-detector circuitry.

10.10.1.2 CIRCUIT DESCRIPTION

The RF power module contains class-A driver amplifiers and high-power class-B amplifiers. Both stages operate in push-pull. Special broadband transformers are used at the output (T2) and the interstage coupling (T1). These transformers are designed to have a substantially level response and low losses over the frequency range 1.6 - 30 MHz.

The driver stages Q1 and Q2 operate class AB with conventional biasing through the current source transistor Q7. The 50-ohm output from the exciter is matched to the base through the broadband transformer T3. Collector-base feedback is provided by the networks C2/R2/L3 and C3/R3/L4.

The output stage is the push-pull transistors Q3 and Q4. The transformer T1 provides the correct impedance transformation from Q1 and Q2 to the bases of Q3 and Q4. C28/R5 and C29/R9 are the collector-base feedback networks together with one turn of inductive coupling through transformer T2. The stabilization of the bias supply is important in a high-power output stage as the emitters of Q3 and Q4 are grounded and the base circuit draws substantial current at high-power output. The dc-coupled transistors Q5 and Q6 form a stable bias regulator. The final amplifier resting current is set by R6. The bias regulators are mounted on the heatsink in close proximity to Q3 and Q4. This means that the thermal characteristics of all devices track closely and the bias current remains stable over the entire operating range of the amplifier.

The dc supply voltage is supplied to Q3 and Q4 in both the transmit and receive modes to prevent voltage drop in the switching circuitry. The driver stages Q1 and Q2 and the bias regulator are supplied from the regulated transmit +12-V line. This means that the driver is off in the receive mode and the final amplifier cannot draw current as there is no forward bias.

10.10.2 BIAS ADJUSTMENT

Final transistor bias adjustment needs checking only after the replacement of Q3 and Q4. Insert a meter in the supply lead to the final amplifier (1000 mA scale). Press the push-to-talk switch, taking care not to operate in the AM mode, or to speak into the microphone. Adjust R6 until the resting current is approximately 300 mA. This is not a critical adjustment.

Driver transistor bias can be checked by inserting a meter in series with the T+ input to the module. Key-down, no signal, current should be 1.0 A, ±100 mA at this point (this results in a Q1/Q2 quiescent current of approximately 200 mA). This current can be adjusted, if necessary, by changing the value of R23; a lower value of R23 raises the bias while a higher value lowers it.

10.10.3 VOLTAGE CHART

Table 10.10-1 defines relevant voltages for the RF power module, M10.

10.10.4 SERVICING

The first check is to ensure that the fault is in the RF power module and not in the exciter or the RF filters. First check the RF voltage (approximately 70 V RMS) at the output of the module. This is conveniently checked at the standoff insulator at the top left corner of the module. Next, check the voltage at the 50-ohm load. If there is a big voltage differential, the fault is in the RF filter module M7 or in the connections between M7 and M10 or M7 and the antenna terminal.

The output from the driver module M4 should be checked, or alternatively the module M10 can be checked using a signal generator as shown in the diagram. If the signal generator is used with AM modulation, the linearity of the amplifier can be checked using an oscilloscope, by comparing the audio waveform on the RF waveform at the input and output of the module. Except for the amplitude, the waveforms should be identical if there is no distortion in the amplifier.

The amplifier should show approximately the output indicated in Table 10.10-2.

The driver stage is usually operating correctly if the dc voltages are correct at Q1 and Q2. A quick check of the stage can be made by checking the voltage at the base and collector using the oscilloscope. There should be substantial gain in the stage.

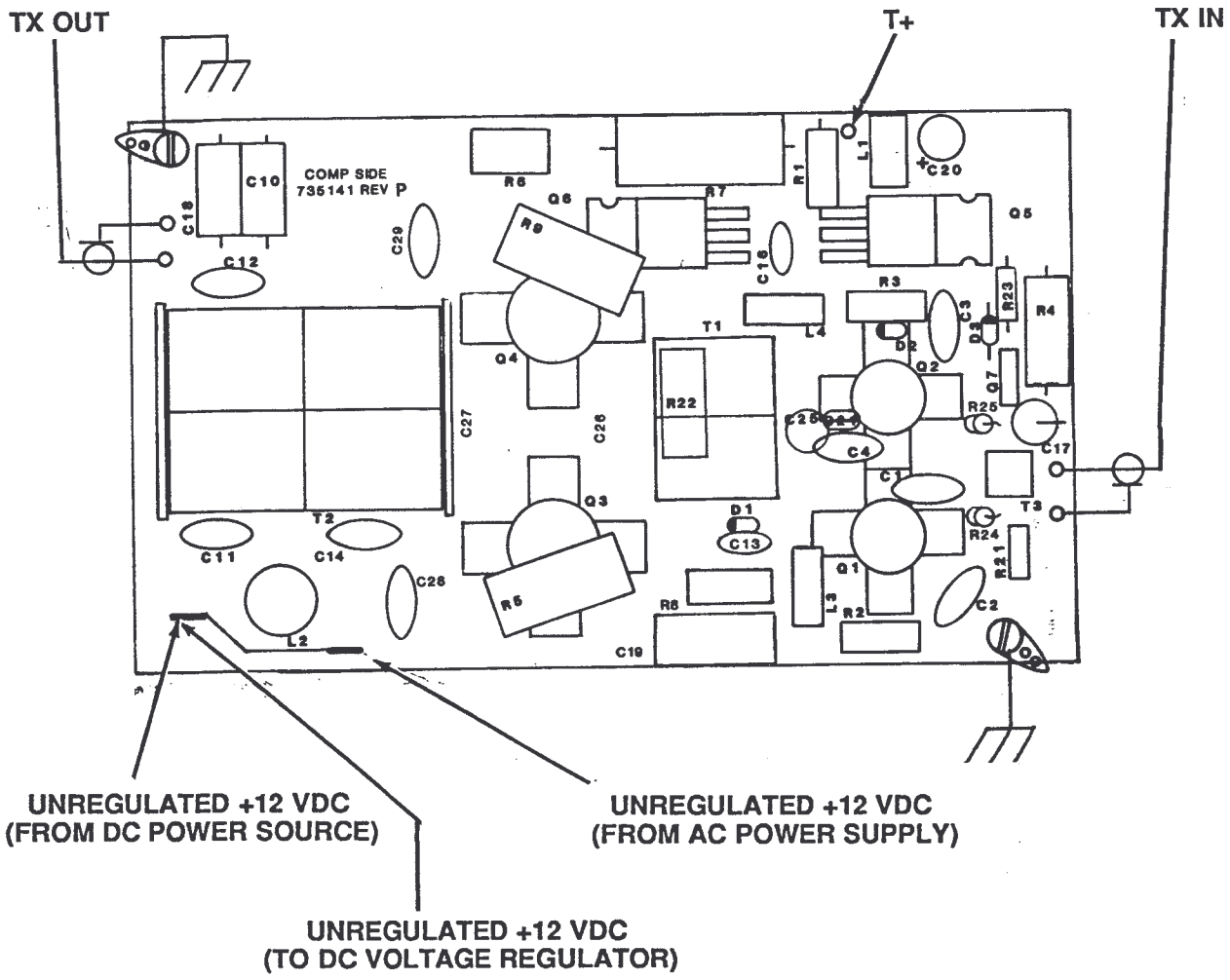


FIGURE 10.10-1.
M10 PCB Interconnections.

TABLE 10.10-1.
Voltage Chart, RF Power Module, M10.

Q1 & Q2		Emitter:	Grounded	
		Collector:	12.0 V	
		Base:	0.7 V	
Q3 & Q4		Emitter:	Grounded	
		Collector:	14.0 V (nominal)	
		Base:	0.7 V	
Q5		Emitter:	0.7 V	
		Collector:	8.0 V	
		Base:	1.4 V	
Q6		Emitter:	0.1 V	
		Collector:	1.4 V	
		Base:	0.7 V	
Q7		Emitter:	0.7 V	
		Base:	1.4 V	
		Collector:	12.0 V	
U1				
Pin 1	3.0 V	Pin 5	0.0 V	No Signal Voltages
Pin 2	18.0 V	Pin 6	0.0 V	
Pin 3	18.0 V	Pin 7	18.0 V	
Pin 4	0.0 V	Pin 8	18.0 V	

A failure in the push-pull amplifier stage Q3 and Q4 is usually self-evident. Component failure usually results in overheating and discoloration of the part. If the voltages are normal and there is no output, one of the transistors Q3 or Q4 has probably failed. It is important to remember that the output transformer T2 does not have coupling between the two primaries; and if one transistor fails, there will be very little output.

The bias circuit is defective if there is no voltage on the bases of Q3 and Q4. This will not prevent the final amplifier from operating, but there will be severe crossover distortion and reduced output. The dc measurements in the bias circuit will usually indicate the defective transistor or component.

CAUTION

1. When replacing final amplifier transistors, they must always be replaced in matched pairs or using a transistor from the same beta group. The beta group is marked on the ceramic body by a color dot.

2. Refer to Section 8.6.6 before replacing the transistor. The RF power transistors are expensive devices and incorrect mounting techniques may result in damage to the device or thermal failure.

TABLE 10.10-2.
Output, Amplifier.

INPUT LEVEL	FREQUENCY	POWER OUTPUT
0.3 V	2 MHz	80 W
1.0 V	15 MHz	80 W
2.0 V	30 MHz	80 W

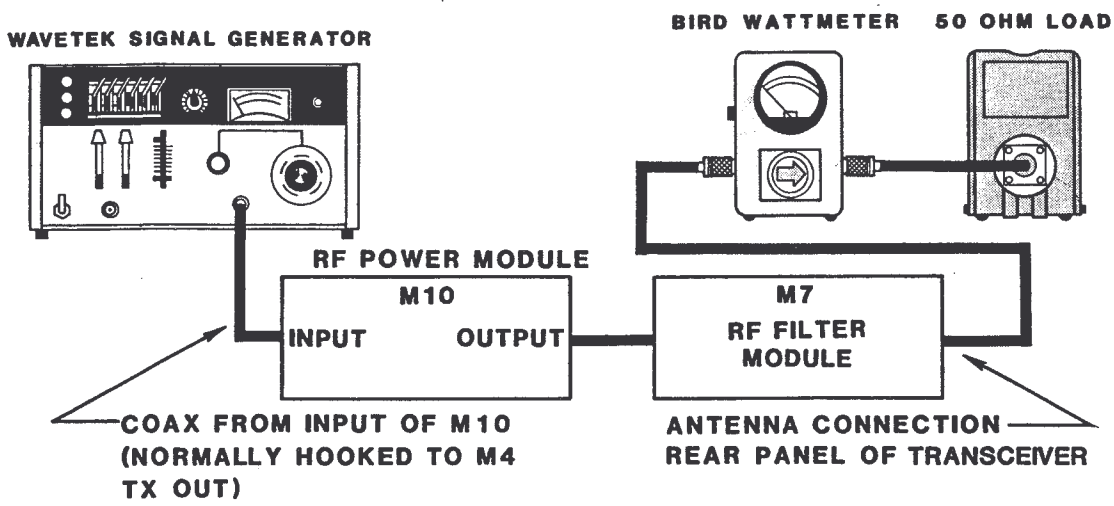


FIGURE 10.10-2.
Power-Module Test Setup.

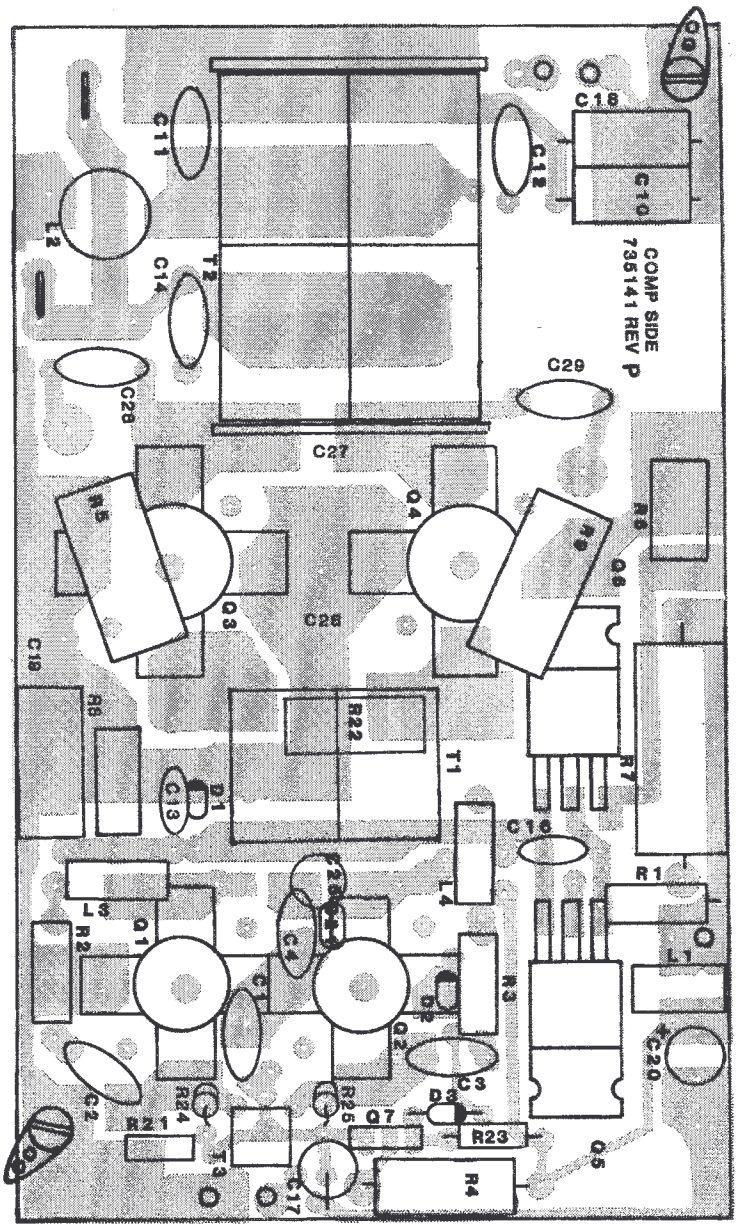
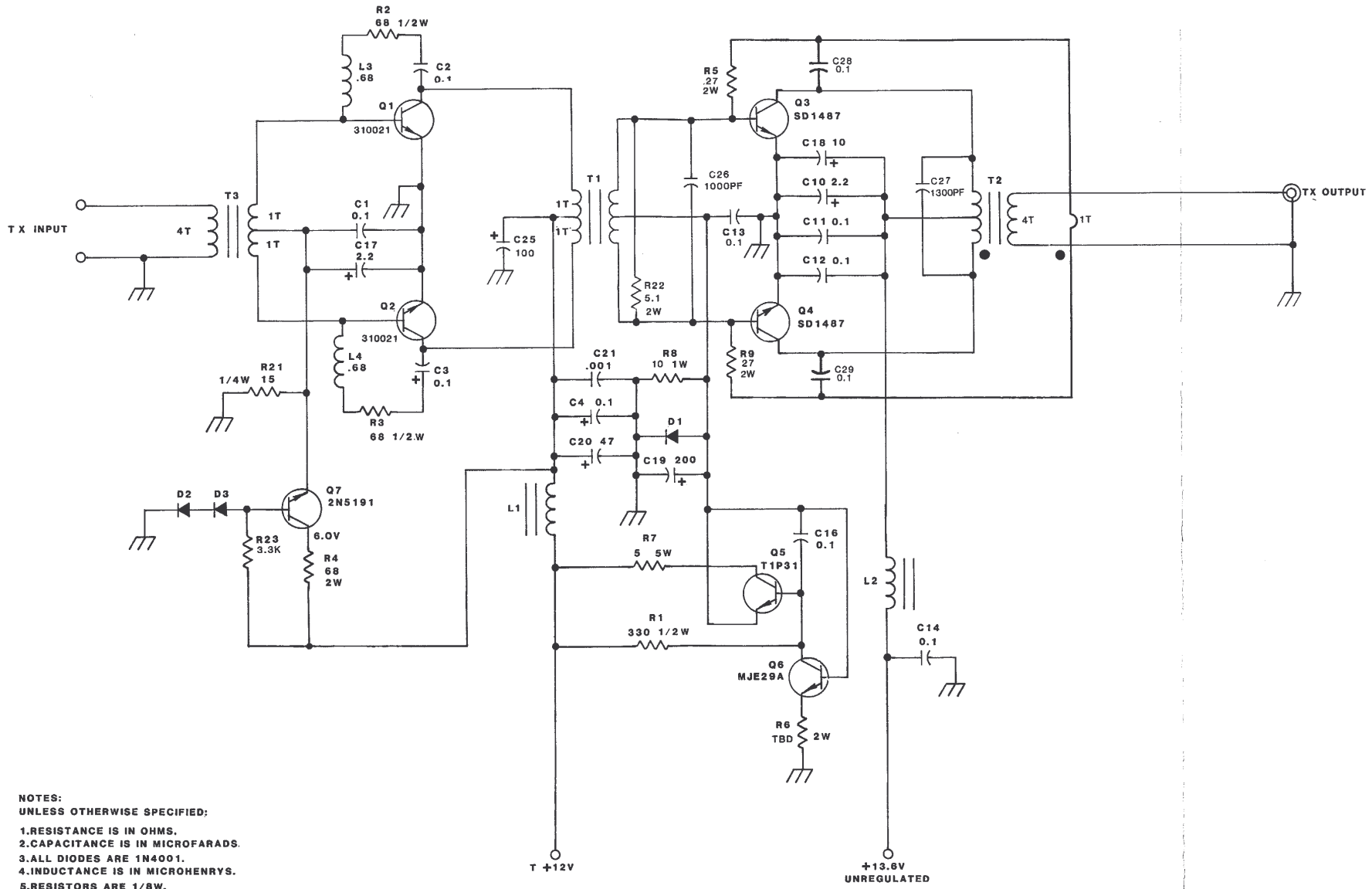


FIGURE 10.10-3.
Component Locations, RF Power Module, M10.



NOTES:
UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE IS IN OHMS.
2. CAPACITANCE IS IN MICROFARADS.
3. ALL DIODES ARE 1N4001.
4. INDUCTANCE IS IN MICROHENRYS.
5. RESISTORS ARE 1/8W.

TABLE 10.10-3.
Parts List, RF Power Module, M10.

C1-C4	210104	Capacitor, Disc 25 V 0.1 μF
C5-C9		Not Used.
C10	230020	Capacitor, Electrolytic 2.2 μF
C11-C14	210104	Capacitor, Disc 25 V 0.1 μF
C15A, C15B		Not Used.
C16	210104	Capacitor, Disc 25 V 0.1 μF
C17	231020	Capacitor, Electrolytic 2.2 μF
C18	230100	Capacitor, Electrolytic 10 μF
C19	230201	Capacitor, Electrolytic 200 μF
C20	231500	Capacitor, Electrolytic 47 μF
C21	210102	Capacitor, Disc 0.001 μF
C22-C24		Not Used.
C25	231101	Capacitor, Electrolytic 100 μF
C26	218102	Capacitor, Chip Ceramic 500 V 1000 pF
C27	218132	Capacitor, Chip Ceramic 500 V 1300 pF
C28, C29	275104	Capacitor, Monolithic 50 V 0.1 μF
D1-D3	320102	Diode, 1N4001
D4		Not Used.
L1	450133	Inductor, Ferrite
L2	450134	Inductor, Ferrite
L3, L4	430005	Inductor, Fixed 0.68 μH
Q1, Q2	310021	Transistor, RF HF 30 W
Q3, Q4	310071	Transistor, RF PWR 100 W
Q5	310023	Transistor, NPN TIP31
Q6	310024	Transistor, MJE29A
Q7	310055	Transistor, NPN 2N5191
R1	135331	Resistor, Wirewound 1/2 W 10% 330 Ω
R2,R3	134680	Resistor, Film 1/2 W 5% 68 Ω
R4	154680	Resistor, Film 2 W 5% 68 Ω
R5	164270	Resistor, Film 5 W 5% 27 Ω
R6	TBD	Resistor, Film 2 W 5% TBD
R7	161050	Resistor, Wirewound 5 W 10% 5 Ω
R8	144100	Resistor, Film 1 W 5% 10 Ω
R9	164270	Resistor, Film 5 W 5% 27 Ω
R10-R20		Not Used.
R21	124150	Resistor, Film 1/4 W 5% 15 Ω
R22	154051	Resistor, Film 2 W 5% 5.1 Ω
R23	124332	Resistor, Film 1/4 W 5% 3.3 kΩ
T1	451134	Transformer 2:1
T2	451135	Transformer 4:1
T3	459126	Transformer 4:2
U1		Not Used.

10.11 LCD DISPLAY, M11

The LCD display is attached to the M11 PC board. The two display driver IC's are located on the board, and it also serves to mount up to three ancillary push-button switches in the TW100F. The module takes its +5-V supply from the M9 module.

The display drivers are CMOS, ultra-low current devices. They are 32-bit serial-in, parallel-out shift registers which have the ability to have their outputs complemented (inverted) under control of an external signal. The only other component on the module is a 0.1-microfarad bypass capacitor.

10.11.1 CIRCUIT DESCRIPTION

The M11 module is powered and controlled by the M9. The input lines consist of the two supply lines, a data line, a clock line, and a backplane input. The supply voltage is +5 Vdc and the supply current at ambient temperature is about 2 microamps, so the power consumption of M11 is an extremely low 10 microwatts.

The data line and clock line provide for the serial inputting of data to the drivers. A total of 64 serial bits must be shifted in each time the display is updated. The data will be valid on the rising edge of the clock. The clock pulse duration is roughly 10 microseconds and is not critical. See the M9 description for more information on the serial format.

The LCD requires a backplane signal to operate properly. The signal must be as nearly a square wave as possible, and its frequency must be within certain limits. The M9 provides a 20- to 60-Hz square wave for this purpose. This signal, known as the "T/C" line (for TRUE/COMPLEMENT), is also connected to the invert control pin of the drivers.

Segments which are off are driven by the noninverted backplane signal. By driving the invert control pin of the drivers with the backplane signal, each output bit which is a zero (0) will follow the backplane signal, and ones (1) will be the inverted signal desired to turn the segment on. So, by shifting in the right combination of data, any display may be shown.

In the flyaway transceiver, the "SCAN," "UP," and "DOWN" buttons are mounted on the M11 and are scanned as part of the keypad polling procedure. The buttons are wired to the M9 along with the keypad harness.

10.11.2 TEST PROCEDURE AND TROUBLESHOOTING GUIDE

Refer to sections 10.9.3 and 10.9.4 for the Test Procedure and Troubleshooting Guide applicable to the M9 and the M11 modules.

TABLE 10.11-1.
Parts List, Microprocessor Display Module, M11.

LCD	320802	LCD, 6 Digit
U1, U2	330148	IC, MD4332B

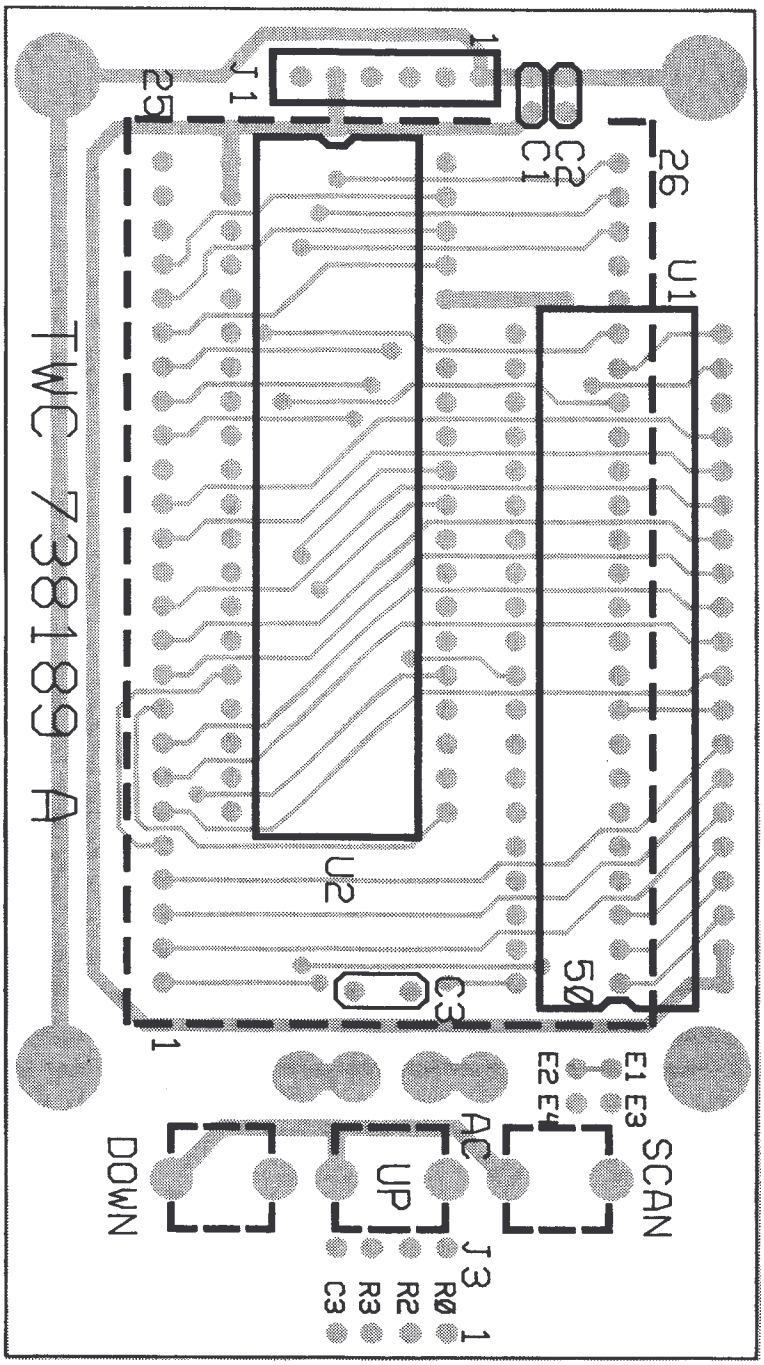
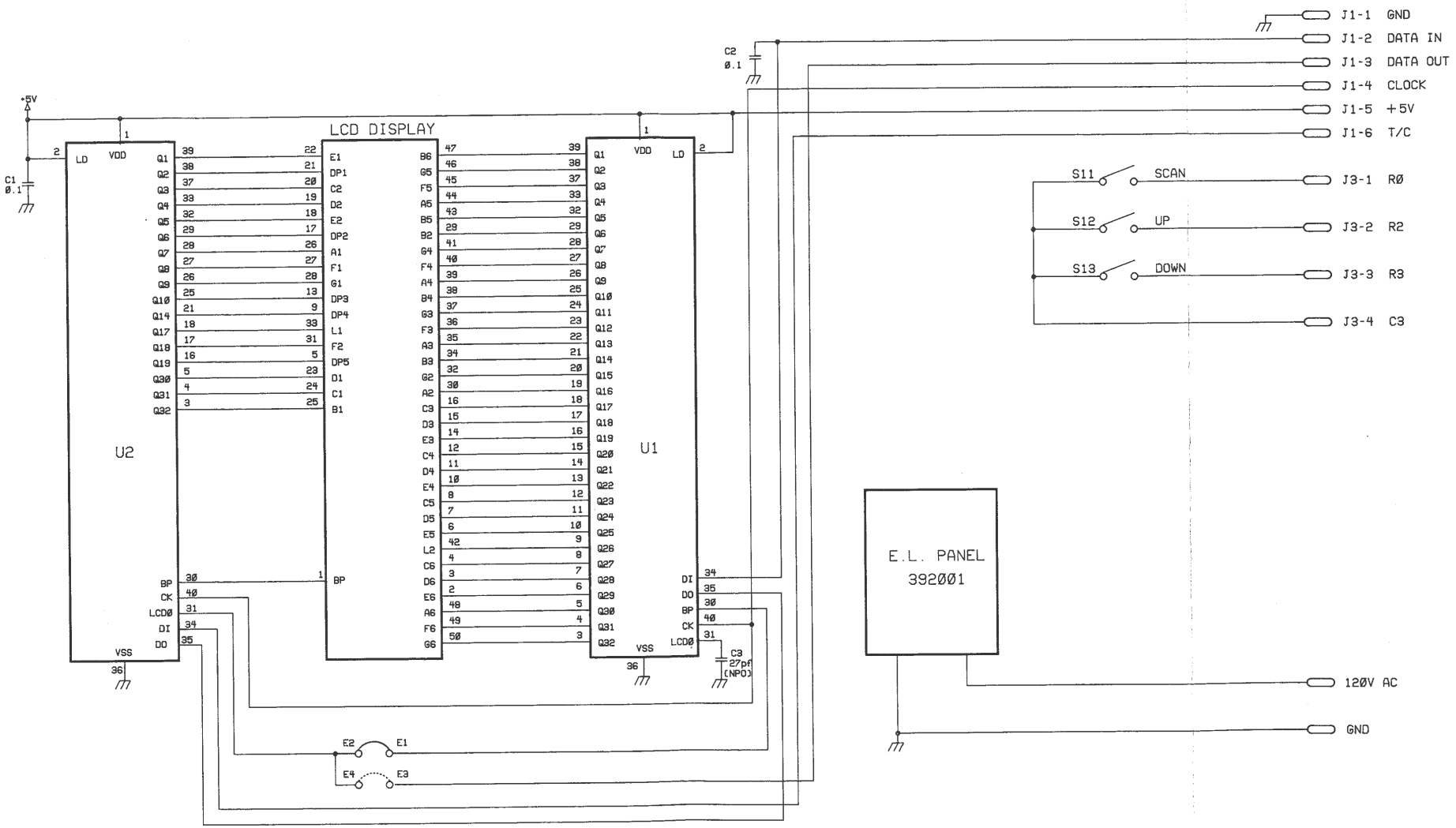


FIGURE 10.11-1.
Component Locations, LCD Display, M11.



6 FOR RT1ØØ-M11 DISREGUARD
S11, S12, S13, AND J3
5 TW1ØØF-M11 SHOWN
4 INDUCTANCE IS IN MICROHENRYS
3 DIODES ARE 1N4148

10.12 TECHNICAL DESCRIPTION - ANTENNA TUNER

10.12.1 CIRCUIT DESCRIPTION

The antenna tuner is a modified L-section matching network. The 50-ohm output from the transceiver is applied through S10 to the matching transformer T2. This transformer has two stepdown ratios—2:1 and 3:1. S10 can select no transformation, a 2:1 or 3:1 impedance stepdown or—by reversing the transformer—a 2:1 impedance step-up. This gives output impedances of 6 ohms, 12 ohms, 50 ohms and 200 ohms. The series-tuning element consists of 16 toroidal inductors connected in series to provide a total inductance of 22 microhenries. A high-voltage ceramic switch, S11, selects these inductors in turn, to give 0-22 microhenries in 17 progressive steps. The shunt output capacitor C3 is a high-voltage 100-pF variable capacitor.

The L network, consisting of L1 and C3, provides an upward impedance transformation. Most antennas exhibiting capacitive reactance have a resistive component of less than 50 ohms, and the network is operated with C3 at minimum setting. The capacitive reactance of the antenna is cancelled by the appropriate series inductance, which gives a resistive termination. The input transformer tap providing the closest match is selected. In practice C3, the shunt capacitor, is also used to provide vernier adjustment between the impedance and inductive taps. Antennas having inductive reactance usually have a resistive component higher than 50 ohms. The antenna can usually be matched by providing a combination of reactance cancellation and impedance step up using C3 and L1. The use of the input transformer with four ratios much reduces the transformation ratios required in the matching network and makes practical a very small, efficient, high-power antenna tuner that is simple to use.

The antenna tuner is permanently connected to the 50-ohm antenna connector. The input transformer is switched to the 50-ohm straight-through position and the minimum capacitance and inductance positions are selected. If the 50-ohm antenna is not a good match, the antenna tuner may be used to provide a low VSWR to the transceiver. The antenna tuner is also operative in the receive mode and matches the antenna to the transceiver.

There are some limitations on the antennas that can be used with the tuner. Very short antennas would require large inductors. The tuner would generate very high voltages, which makes it impossible to incorporate the tuner inside the transceiver. The tuner requires a minimum antenna length of 7.5 m for operation down to 3 MHz and 15 m for operation from 2-30 MHz. The antenna tuner may not have sufficient range for very long antennas. A supplementary 50-pF capacitor is provided in the antenna kit for insertion in series with the antenna connector and the antenna for use with these antennas.

The antenna tuner has no internal adjustments and requires no routine maintenance. The components are all heavy-duty and should only require replacements if mechanically damaged. Check that the capacitor plates are not bent and that the shaft rotates smoothly. The inductor can be checked by placing the switch in the maximum inductance position and checking with an ohmmeter for continuity. If there is an open circuit, locate the faulty inductor and repair. The input transformer uses teflon wire in the secondary, and brass tubes in primary. Defects are unlikely to occur. Since the voltages in the tuner can be very high, it is important to keep the components clean.

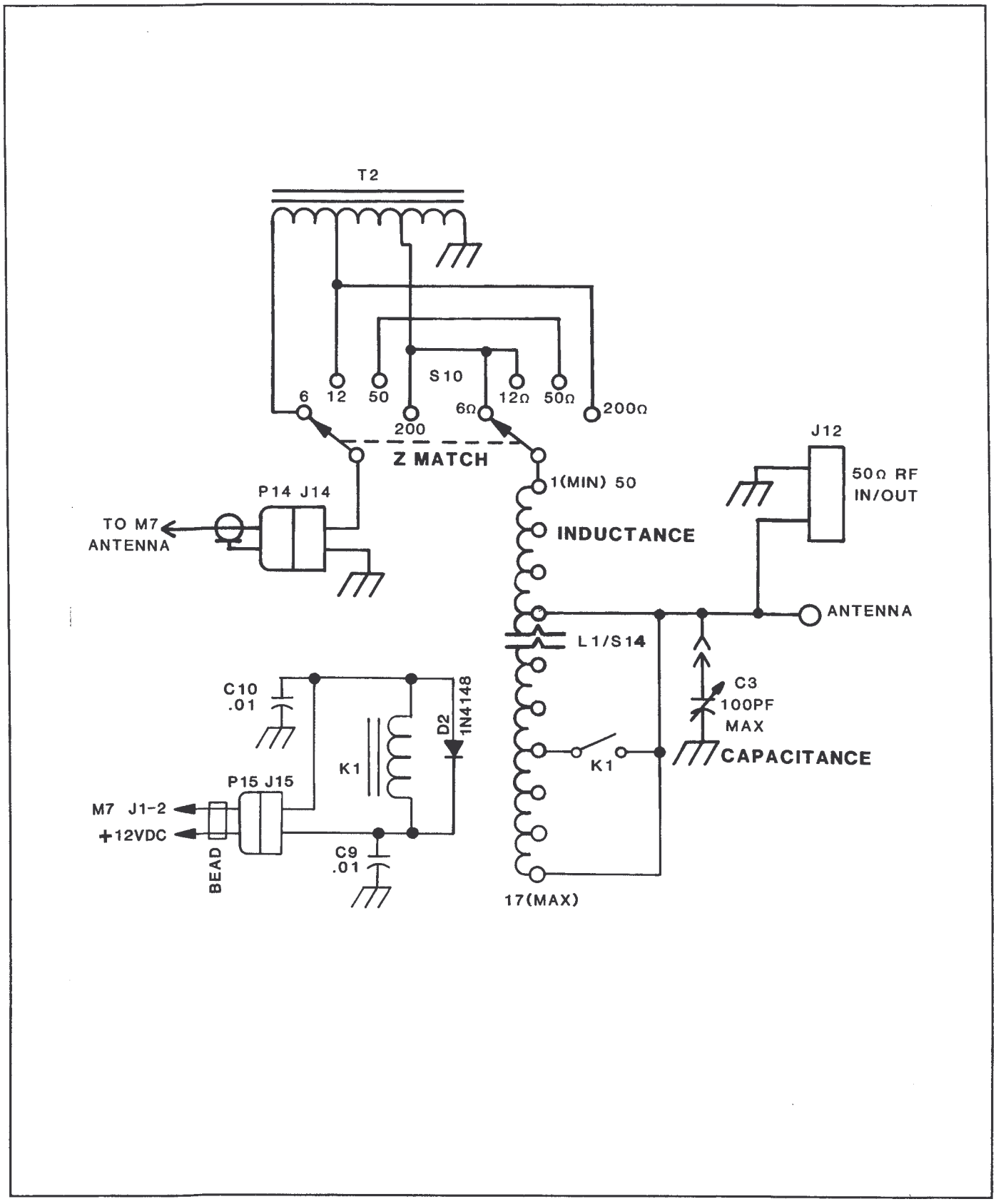


FIGURE 10.12-1. Schematic Diagram, Antenna Tuner, M12.

SECTION 11
CHASSIS/MAINFRAME

11.0 MAINFRAME

This section contains information on the chassis- and mainframe-level components not covered elsewhere as well as the overall wiring and accessory connector configurations. Figure 11-1 defines the top-view module locations; Figure 11-2 defines the bottom-view module locations. Table 11-1 defines the various accessory-connector configurations. Figure 11-3 is the mainframe schematic diagram and the parts are defined in Table 11-2.

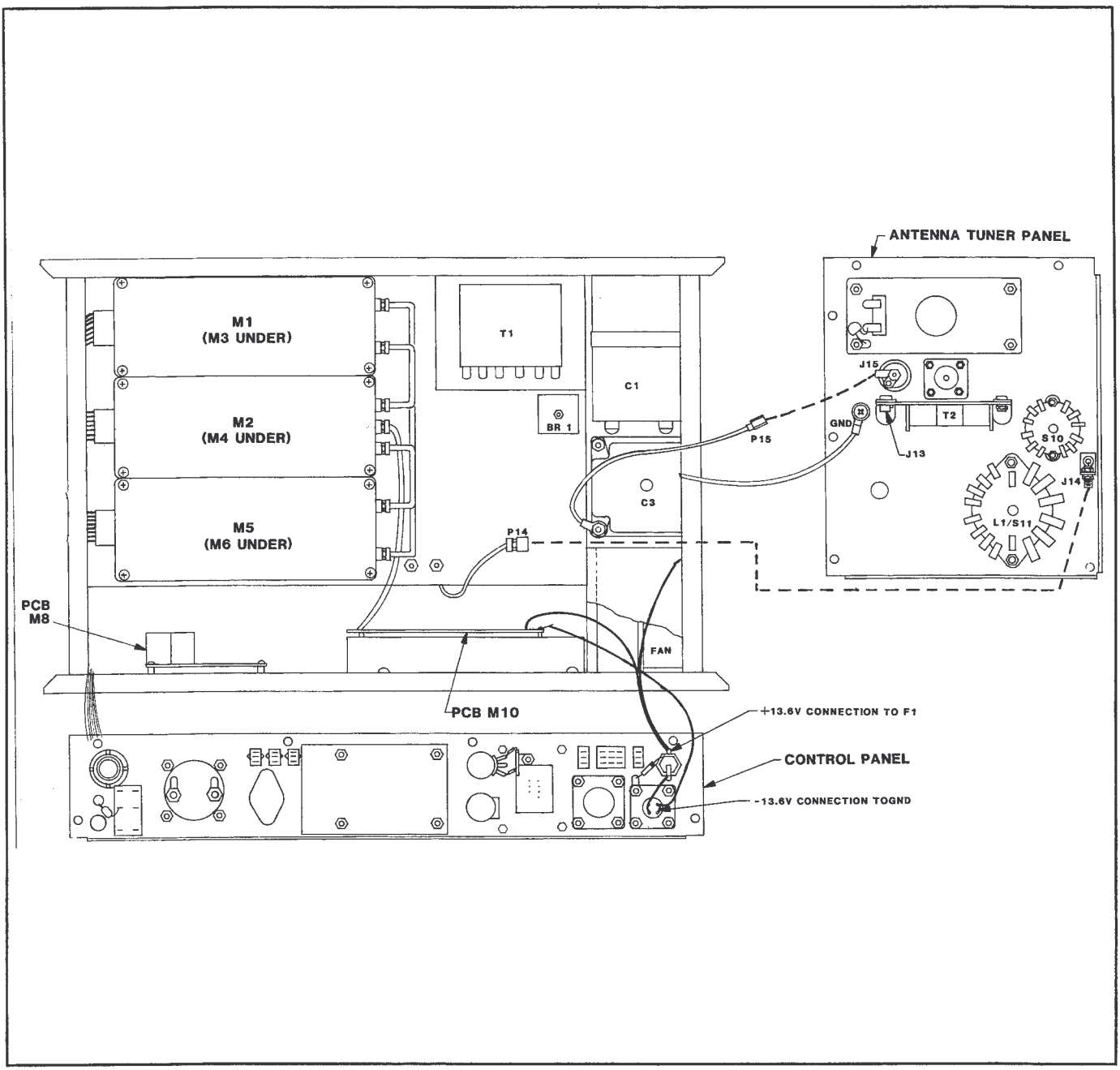


FIGURE 11-1.
Module Locations, Top View.

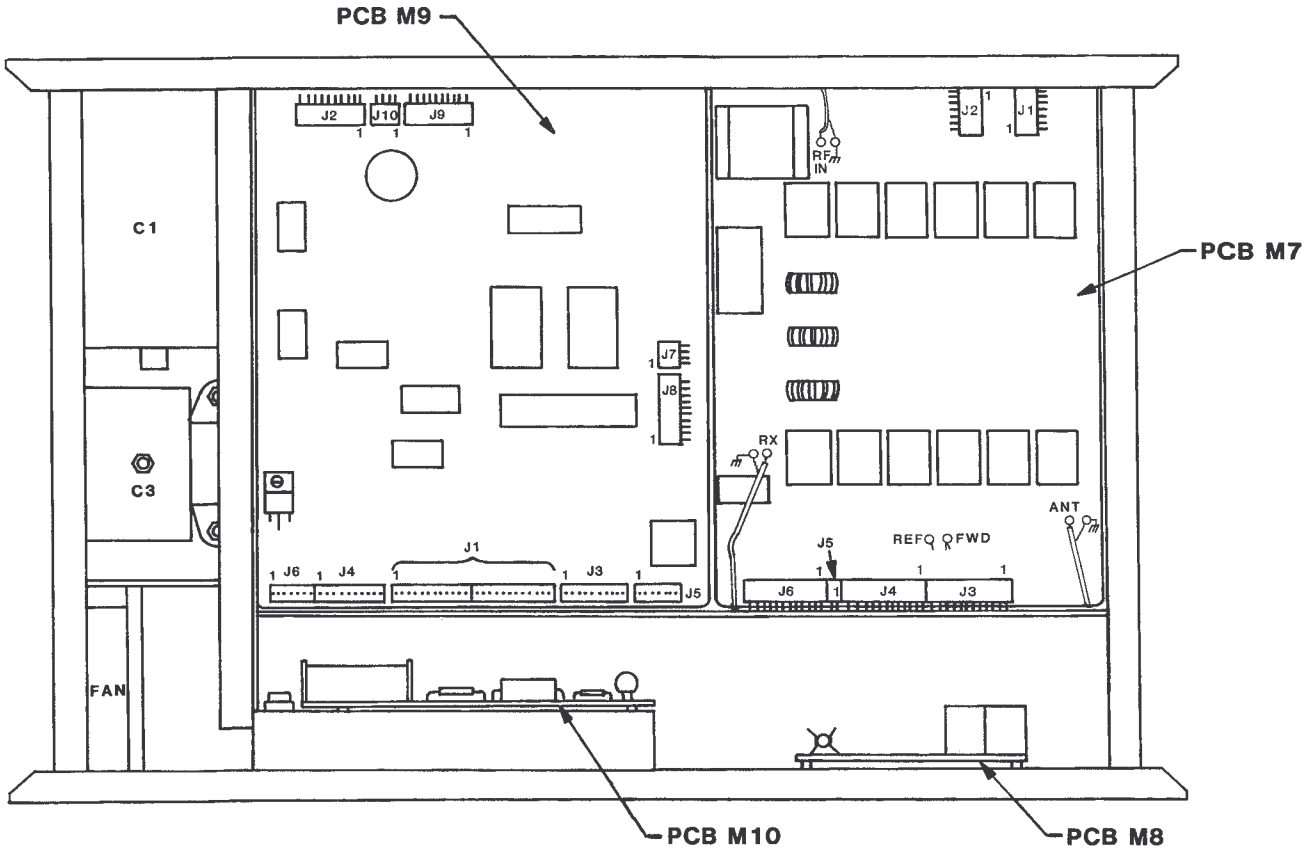
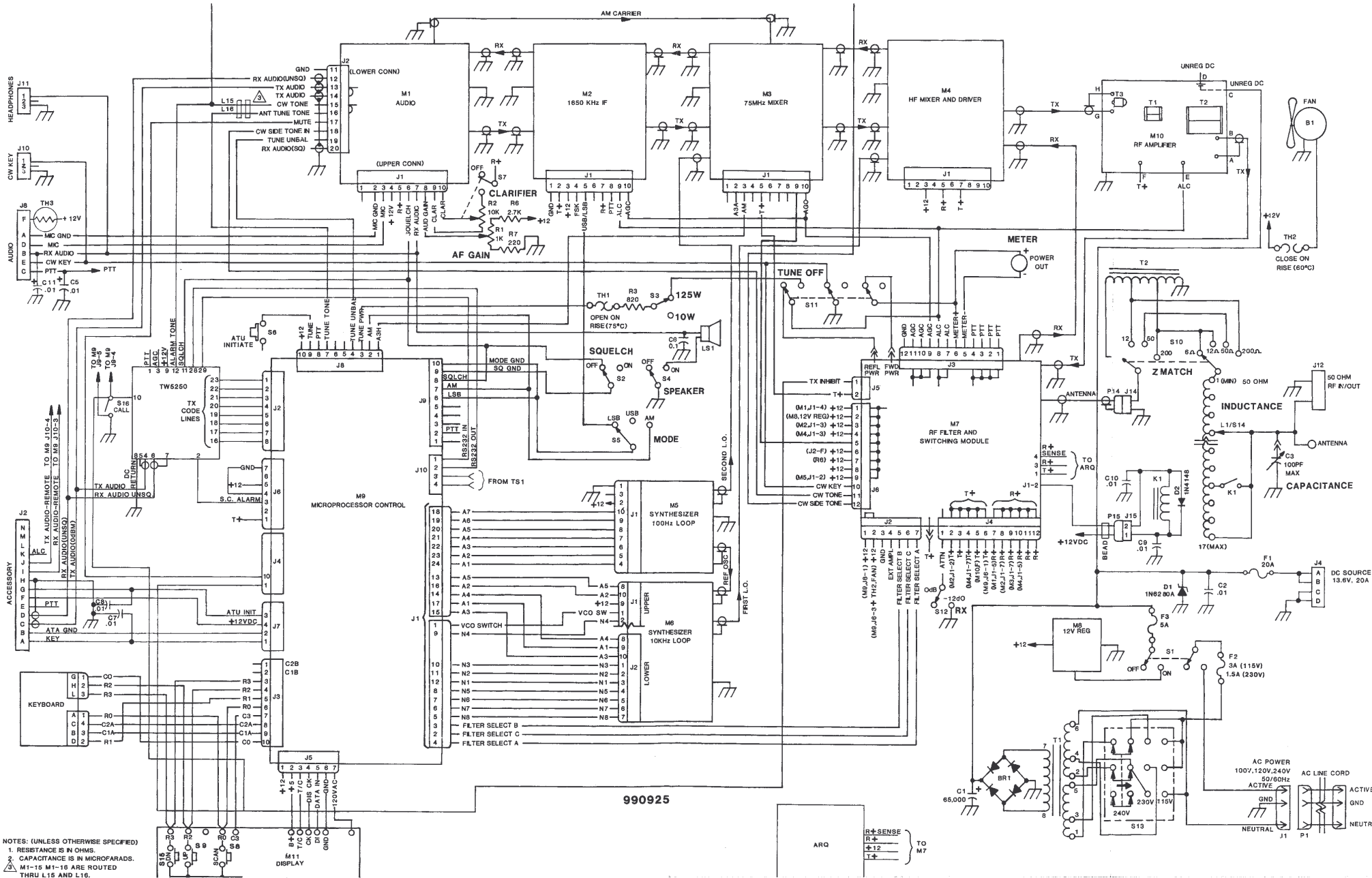


FIGURE 11-2.
Module Locations, Bottom View.

TABLE 11-1.
Pin Assignments - Accessory Connector, J2.

J2	MP
A	Key
B	Ground
C	TX Audio (0 dBm)
D	RX Audio (UNSQ)
E	PTT
F	+12 Vdc
G	ATU Initiate
H	Ground
I*	Remote Control (RX Audio) } 4-Wire
J*	Remote Control (TX Audio) } Remote
K	ALC
L	Spare
M	Spare
N	Spare

***The Remote Control wires may be reconnected for RS232: Pin I—RS232 IN; Pin J - RS232 OUT.**



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTANCE IS IN OHMS.
2. CAPACITANCE IS IN MICROFARADS.
3. M1-15 M1-16 ARE ROUTED THRU L15 AND L16.

TABLE 11-2.
Parts List, Mainframe.

B1	770005	Fan, 12 Vdc
BR1*	320501	Diode Bridge 35 A 100 V
C1*	230653	Capacitor, Electrolytic 25 V 65000 µF
C2	214103	Capacitor, Monolithic 50 V 0.01 µF
C3	264101	Capacitor, Air Variable 100 pF
C4		Not used.
C5	214103	Capacitor, Monolithic 50 V 0.01 µF
C6	210104	Capacitor, Disc 0.1 µF
C7-C11	214103	Capacitor, Monolithic 50 V 0.01 µF
D1	320225	Diode, Zener IN6280A
D2	320002	Diode, 1N4148
F1	550010	Fuse, 3AG 20 A
F2	550003	Fuse, 3AG 3 A (115 V)
	550018	Fuse, 3AG 1.5 A (230 Vac)
F3	550005	Fuse, 3AG 5 A
J1	610401	Connector, Ac Power
J2	613046	Connector, Accessory
J3		Not Used.
J4	613004	Connector, Dc Power
J5		Not Used.
J6		Not Used.
J7		Not Used.
J8	613090	Connector, Audio
J9		Not Used.
J10	660004	Connector, CW Key
J11	660002	Connector, Headphones
J12	610003	Connector, 50 Ohm, RF IN/OUT
J13		Not Used.
K1	540021	Relay, Reed 12 Vdc
L1/S14	920329-1	Inductor, Switch Assembly
L15,L16	490302	Bead, Ferrite
R1	170020	Potentiometer, Linear 1 kΩ
R2/S7	170007	Resistor, Control Audio DPST 10 kΩ
R3	113821	Resistor, Film 1/8W 5% 820 Ω
R4,R5		Not Used.
R6	124272	Resistor, Film 1/4W 5% 2.7 kΩ
R7	124221	Resistor, Film 1/4W 5% 220 Ω
S1	520018	Switch, Power
S2	520001	Switch, Squelch, SPST
S3	520001	Switch, High/Low Power
S4	520001	Switch, Speaker On/Off SPST
S5	510019	Switch, Mode
S6	530015	Switch, ATU Initiate (optional)
S7/R2	170007	Switch, Clarifier On/Off
S8	530024-4	Switch, Scan Button
S9	530024-5	Switch, Up Button
S10	510036	Switch, Z Match

TABLE 11-3.
Parts List, Mainframe, Continued.

S11	520002	Switch, Tune Off
S12	520001	Switch, RX (Attenuator)
S13	530410	Switch, Transformer Tap
S14	510037	Switch, Inductance
S15	530024-6	Switch, Down Button
S16	530024-9	Switch, Call Button (optional)
T1	410026	Transformer 115/230 14.5 V 12 A
T2	920328-1	Transformer, RF
TH1	560001	Thermostat, NC 75° C
TH2	560002	Thermostat, NO 60° C
TH3	350111	Thermistor, 5 Ω @ 25° C

SECTION 12
TRANSCEIVER INTERNAL OPTIONS

12.0 INTRODUCTION

Standard equipment on the transceiver includes USB, AM, CW, +12-Vdc and 115/230-Vac operation, and a built-in antenna tuner. This section covers other internal features that can be added to the transceiver at the customer's request. These optional features are listed below.

SECTION	INTERNAL OPTION	DESIGNATION
12.1	Remote-Control Interface	RC
12.2	Selcall and Transcall Option	SC & TC
12.3	Wideband Filter Option	WB
12.4	ARQ Option	ARQ

12.1 REMOTE-CONTROL OPTION

12.1.1 GENERAL

The M9RC PCB that is used with the remote control differs significantly from the M9MP PCB used when the remote is not fitted. The local panel control portion remains the same however, except for the fact that the reset and power-up sequence is altered. Everything contained in the basic M9 Section is still valid, including the antenna-tuner interface information, but the following description augments the basic functional description.

The remote control portion of the M9 is comprised of very similar circuitry to the local portion, but also includes a parallel-to-serial data converter (UART) and a modulator/demodulator (MODEM), as well as other interface components.

The remote control achieves its reliability from the fact that it utilizes an "Acknowledge Request" system (ARQ) to make sure that the data displayed on the remote-control head is valid. The system also prevents disruptions on the balanced line from interfering with control.

The control information is sent using an Audio Frequency Shift Keying (AFSK) transmission standard, Bell 103. The data rate is 600 bits-per-second (Baud); a 2225-Hz tone represents a mark or a one (1), and a 2025-Hz tone represents a zero (0). The actual control information is sent in four-byte bursts of eight bits per byte. The first two bytes of any control burst are always fixed. The second two bytes constitute the control information. For every control packet received by the transceiver (telling it to go and do something), an answer-back burst is sent to the head. The answer-back consists of four bytes also, but is inherently twice as easy to receive ungarbled as the control information.

12.1.2 CIRCUIT DESCRIPTION

12.1.2.1 CO-PROCESSING ARRANGEMENTS

As stated above, the local processor and its circuits remain very much as before. The basic difference in the CPU arrangement is that there is now another CPU and some other components on the bus. The additional CPU, known as the Remote CPU, and its support components reside on and share the bus with the other local parts. A circuit tells each CPU when it is its turn to become bus master, and when each should shut down.

When one of the CPU's is to become the bus master, it is told by the arbitration circuit to turn on and begin executing instructions. The other CPU is told to "go to sleep," and ceases to function. The arbitration circuit is simply a flip-flop composed of sections of U29, a quad two-input NOR.

C35 and R36 form a time constant which assures that after power-on the flip-flop is set, putting a high logic level (+5 V) on U29-11. This places operating voltages on U18, the Remote or Master processor. The master/slave relationship of the processors is discussed in 12.1.1.12.

By placing 5 V on the reset and VDD lines of U18 (pins 4 and 26 respectively), U18 is allowed to turn on and begin executing instructions. The effect of this is said to place the circuit in the "remote" or "master" mode.

12.1.2.2 POWER-UP SEQUENCE

The first thing the remote processor does, after turning on, is to initialize the Universal Asynchronous Receiver-Transmitter (UART). This device, U20, is responsible for receiving data via the processor data bus and transforming it into a serial data stream according to the initialized format, and "vice versa." The processor writes four control bytes to the device and sets it up to send 600 Baud ASCII; with one stop bit, 8 data bits, and no parity. It sets the Baud rate generator to external, so the part derives its basic clock rate from the 38,400-Hz square wave produced by U24.

All this takes place in a few microseconds after reset. When this task is completed, the remote processor will place a low level on U18-29, which takes the local reset line (U1-4 to which it is tied) to a low logic level (0V), and resets the local processor. It then places a low on U18-28 which resets the flip-flop via U29-1 and 2. The operating voltages are removed from U18, and placed on U1. Then U1 can come on and begin executing instructions. It should be noted that while one processor is on, the other is off and all its lines are in the high-impedance state.

The operating voltages are placed on U1-4 and U1-26 via U29-10 and the local processor comes on and begins executing instructions. From the local mode, operation is just as described in Section 10.9. However, this normal operation may be interrupted by reception of data by the UART. When data are received by the UART, a third mode, arbitration mode, is entered. If the data are not valid, local mode is resumed. Operation is further discussed in 12.1.2.12.

12.1.2.3 REMOTE AUDIO LINK

The transceiver is normally connected to the control head via two unbalanced 600-ohm lines. One represents the receiver audio (RX audio), and the other the transmitter audio (TX audio). The TX audio also carries the signalling commands from the head to the transceiver, and the RX audio also carries the answer-backs from the transceiver.

The lines enter the PC board through inductive low-pass filters composed of L1, L2, C65, and C66. The TX audio feeds the filter/limiter IC, U13.

12.1.2.4 MODEM FILTER/LIMITER

This IC contains an op amp, a switched capacitor bandpass filter, and a comparator. The op amp is driven from the TX audio and has an adjustable gain via R4. R4 is adjusted to give about 4-V p-p output when the control head

TX audio signal is maximum, as from the control signal tone. The op-amp output drives the transmitter audio input port that is allocated for the remote at M1.

This amplified audio signal also drives the MODEM bandpass filter inside the IC. The output of this filter drives a data comparator, the output of which appears at pin 16 of the IC. R7 is adjusted so that the comparator output (RXC) is a 50 % duty-cycle square wave at the filter passband center frequency. This squared audio signal is what the period-counting demodulator wants to see.

The squelched RX audio from the receiver is fed to U27A, an op amp which drives the RX audio line to the head via emitter follower Q10. R34 sets the maximum output level to the head. The modulator also drives U27A via R64, so that the answer-back tones appear on the RX audio line.

12.1.2.5 DEMODULATOR

The demodulator, half of U21, is a period-counting device. It recognizes the square wave at its input, pin 1, and counts the period of each cycle. If the period of the square wave is close enough to that of either a 2225- or 2025-Hz tone, the RXD output is updated after one complete cycle.

The square wave input must have a duty cycle of 50 % plus or minus 4 % for the demodulator to function. Excessive noise or distortions can cause the duty cycle to err. The RXD output drives the RXD port of the UART.

12.1.2.6 MODULATOR

The modulator half of U21 receives its transmit data from the UART on the TXD line. A one (or mark) is converted to a 2225-Hz tone and a zero is made to be a 2025-Hz tone. The tone output at TXC, pin 9, is normally suppressed until it is desired to send a data burst. To start the tone burst, the MUTE line, U21, 12, is set to a one (+5). A delay of about 10 ms is generated, and then the four data bytes are sent. Then the MUTE line is taken back low to stop the data burst.

12.1.2.7 MODEM CLOCK

The basic timing for the MODEM is derived from its crystal oscillator, Y4. It runs at or near 1.00000 MHz. It is not critical that this frequency be closer than 0.1 %. This crystal runs continuously.

12.1.2.8 REMOTE DISABLE

Q16 is a grounded-emitter switch which can effectively ground the RXC input to the MODEM and prevent any audio from reaching the device. When the remote cable is plugged into the accessory connector on the transceiver, the base of Q16 is grounded, and it cannot conduct. The remote circuits are then allowed to function. When the cable is removed, the MODEM cannot receive any data and the remote is disabled.

12.1.2.9 MINUS 12-V SUPPLY

The 12-V supply is not installed in revision AC and later M9RC boards. U24 is an oscillator and divider chain. The oscillator runs at 614.4 kHz as determined by the ceramic resonator, Y5. As stated above, the 38.4-kHz output drives the UART clock inputs. This rate is exactly 64 times the 600-Baud data rate.

The 38.4 kHz also drives a switching power-supply circuit to provide the minus 12 V needed for the RS-232 interface. A toroidal inductor is used with an inductance of roughly 2000 microhenrys. Q11 drives Q12, and Q12 in turn puts current pulses through the inductor during half the cycle. During the other half of the cycle, Q12 is shut off and the field in the toroid is allowed to collapse. This induces a voltage back across the inductor. The magnitude of the induced voltage is inversely proportional to the switching speed of Q12, and also depends on the "Q" of the inductor.

The diode and capacitor form a simple filter and the 2.2-kΩ resistor across C64 provides enough loading to prevent the inductive "fly-back" voltage from being excessively great. Nominally there are about -25 V across C64. This raw voltage feeds a 79L12 minus 12-V regulator.

12.1.2.10 RS-232 INTERFACE

RS-232 is just a name for a set of specifications describing a way to transfer serial data from one point to another. The most important features of the standard are:

1. Signals must swing from above +3 V to below -3 V.
2. A level lower than -3 V constitutes a mark or one (1).
3. A level higher than +3 V constitutes a space or zero (0).
4. Levels in between are undefined.
5. Rise and fall times of signals are limited.

In fact, the RS-232 output from the M9MP is allowed to swing from roughly +10 V to -10 V.

12.1.2.11 RS-232 CIRCUIT DESCRIPTION

The original RS-232 circuitry (PCB 735140 Revision AB and before) is easily spotted by the presence of the 2 mH inductor L3, as described in Section 12.1.2.9. In this configuration the output is current limited by R69. It is driven from half of U25, an op amp which is powered from +12 V and -12 V. The input of the op amp is driven directly from the TXD line from the UART.

The RS-232 input drives the input of the other half of U25 through R68. The non-inverting inputs of both op amps are supplied with a fixed +2.1-V reference which sets the switching threshold. Thus, the RS-232 input will actually accept a 5-V/0-V (TTL) signal and still function.

The output of U25-1 is tied to the RXD line through a 10-kΩ resistor, R61, and a diode, D39. When its output goes to -10V, or space (note that the op amp inverts the incoming signal) the RXD line is taken to 0 V. When the

op amp goes to +10 V or mark, the RXD line is allowed to be pulled up to +5 V by the pull-up resistor, R65.

It should be noted that if the MODEM is enabled by plugging in the accessory connector, RS-232 communications would be disrupted occasionally by the presence of data from the demodulator. If constant RS-232 operation is desired, the remote disable must be set. Remove U21 completely if the audio remote is never to be used.

To convert a "normal" 2- or 4-wire configured M9RC board (PCB 735140 Rev. AB or earlier) to RS-232 operation:

1. Install L3 near Y2 by soldering the inductor leads into the holes provided.

2. Secure L3 with silicone adhesive or a nylon nut and bolt.

3. Swap the wires at M9RC-J10 as follows:
Pin 4 wire goes to pin 1.
Pin 3 wire goes to Pin 2.
(The pin numbers are noted on the PCB.)

The new RS-232 circuitry (PCB 735140 revision AC and later) takes advantage of a single integrated +5-V powered RS-232 driver/receiver, U32, which eliminates the need for a -12-V generator and separate op-amp buffers at J10. This new circuitry supplies and receives the same ± 10 V (approximately) data as the old configuration.

To convert a 2- or 4-wire M9RC (PCB Rev. AC or later) to RS-232 operation:

1. Install U32.
2. Move J10-4 wire to J10-1.
3. Move J10-3 wire to J10-2.

M9RC boards using PCB 735140 Rev. AD or later have provisions for switching both the RX and TX data lines between the modem and the RS-232 port. This modification is required for use with the M5A/1045 Automatic Link Establishment system.

12.1.2.12 CONNECTION TO COMPUTER

The input and output lines are connected to the computer using either a shielded cable or twisted pairs. For long runs, the two twisted pairs are recommended. Ground is paired with a signal line in each pair. Hook the RS-232 output to the serial input of the computer, and the RS-232 input to the serial output of the computer. Most computer serial ports have a busy line which must be tied permanently to one logic level or another for this system to work. This tells the computer that the transceiver is always ready to receive data. A delay must be incorporated in the computer program to allow for the system format.

12.1.2.13 REMOTELY CONTROLLABLE FUNCTIONS, HARDWARE LEVEL

U22 and U23 are responsible for the additional hardware interface necessary to have control of the mode, transmit and receive, and other panel functions. U22 is simply an additional shift register that is attached to the end of the transceiver interface. It is the sixth and last register in what is now a chain of six registers, one feeding the next with the serial data from the processor ports.

Forty-eight (48) bits are shifted out of either processor when it is desired to update the transceiver interface. The first 8 bits to be shifted out are those which will end up in U22. The definitions of these 8 bits are given here:

Bit	Function	Active Level
Q8 (LSB)	PTT	Low to transmit
Q7	SC SEND	High to send
Q6	ATU TUNE	High to tune
Q5	SQUELCH	High to squelch
Q4	AMPLIFIER CTRL	Low for AMP on
Q3	AM	Low for AM
Q2	SIDEBAND CTRL	Low for LSB
Q1	Not Used	

When the M9 is in the remote mode, a high logic level is placed on U22, 15 which allows the outputs to become active. When in the local mode, a ground is placed on that pin which forces the outputs into the high impedance state. In this state they cannot affect transceiver operation.

U23 is a quad analog switch, and allows certain transceiver panel controls to be disabled when in the remote mode. It also controls the S.C. SEND function. When in the local mode, a high level is placed on U23 pins 5, 6, and 13, and the analog switches conduct. This places the commons of the mode and squelch switches on the transceiver panel at ground, and they are operational.

In the remote mode, a low level is placed on those pins, and the analog switches do not conduct, which thereby disables the panel switches. The S.C. SEND function is implemented by causing one of the analog switches to short across the two lines from the selective-call module (SCM) that also runs to the "SEND" switch.

12.1.2.14 BUS ARBITRATION AND OPERATING STATES

The two processors share a master and slave relationship with one another. U18 is the remote processor and is thought of as master. U1 is the local processor and is the slave. The only reasons this relationship exists are:

1. Obviously one of them has to come on first.

2. Since the change from local to remote modes is automatic, the remote processor must be the one to determine which processor is actually enabled at any given time.

The two processors and their individual resources may be thought of as two separate systems which just happen to share the same data and address bus and the same port lines. The only shared system resources on the buses are the address latch, U2, and the system non-volatile memory, U4. Both systems also share access to the transceiver interface, display interface, and certain other port lines.

Only the remote processor can access the UART, and each system has its own program memory. These are the non-shared system resources. The keypad lines (except for the row containing the "F" key) are not shared, since the remote processor has no need to know that information.

After power on, the transceiver is in the local mode. At this point the UART has been initialized, as mentioned above, and is ready to receive data from the head. The UART is also prone to falsing on something that is not really data. So if, when in the local mode, the UART thinks it has received a data byte, it asserts an interrupt by placing a low level on its RXE line.

This also effectively grounds U29 pins 5 and 6, and pins 6 of both processors. This sets the flip-flop, and the remote processor is allowed to come on and begin executing instructions. It sees that the INT line is held low, and so tries to determine the source of the interrupt. If P16 is also low at U18, 33 then the UART was the source of the interrupt. The UART is signalling that it has a character ready to be read by the processor.

The remote processor can select either the RAM, U4, or the UART by asserting P15, or U18-32. When this line is high, the RAM is selected; when low, the UART is selected. Both cannot be enabled at the same time. Either device, when enabled in this fashion, responds to reads and writes via the databus and communicates with the processor. The other device is disabled and sits in the high impedance state.

The CPU reads the data byte from the UART by asserting the RD line, and by placing the correct levels on A0 and A1 of the UART to address the data-holding register. The CPU then compares the received byte with a table to see if it is part of a valid remote command. If it is not a valid byte, the remote CPU puts a low level on U18-30; which resets the flip-flop and permits the local mode to resume without being reset. Instructions resume from the point where they were interrupted by the UART. This state is known as arbitration mode and takes 5 to 10 ms for each interruption.

If the remote CPU determines that all four bytes of a valid command have been received, it does not return to local mode, but enters remote mode, and outputs the display, "R.C. ON" to the local display. It sends the answerback signal to the head to indicate that a valid command was received.

While in the remote mode, if an interrupt occurs and it is determined that the source of the interrupt is the local "F" key being pressed, the remote CPU outputs a long string of data to the head to indicate that it is returning to the local mode. The control head recognizes this signal and puts up the display, "R.C. OFF" on the head.

The remote CPU then places a low level on U18-29 to reset the local CPU. A delay is generated in software to allow time for the local reset capacitor to discharge through the limited sink capability of the port line. It then asserts U18-30 as above and grants control to the local CPU.

The data used to indicate to the head that local control is resuming are the same fixed value bytes that are used in the acknowledgement signal. This means that if there are two or more control heads in parallel on the balanced line to the transceiver, the following will occur. If one head asserts control, the other will hear the answerback signal and display "R.C. OFF;" since the latter knows it was not the one that sent the data burst in the first place.

TABLE 12.1-1.
M9RC Remote Control Module, Test Procedure.

LOCATION	SEQUENCE NUMBER	PROCEDURE
Transceiver	1.	Make a visual inspection for any missing or wrong components, solder bridges, incorrect wiring, etc.
Transceiver	2.	Make an ohm check from the +12-V line to its ground. The reading should show several hundred ohms.
Transceiver	3.	Apply ac power.
Transceiver	4.	Verify that the LCD backlight comes on and that there is at least 135 V p-p (ac) at the "ac" terminal of the display module (M11).
Transceiver/Control Head	5.	Connect the actual cable to be used from the transceiver to the head. Connect the transceiver RF output to a 30-dB power pad, and the output of the pad to an RF signal generator.
Transceiver	6.	Press the "F" button on the transceiver and change to channel "00".
Transceiver	7.	Tune to a convenient frequency and inject a -30 dBm RF CW signal to the set so that a 1-kHz tone is present. IMPORTANT!! DO THIS AND ALL TESTS THROUGH A 30-dB POWER PAD!! Turn R4 fully CCW.
Transceiver	8.	Monitor the emitter of Q10 with an oscilloscope set to 1 ms/div and 2 V/div ac coupled.
Transceiver	9.	Adjust R34 until the sine wave is 12 dB under the clipping threshold. Verify that this about 2.5 V peak-to-peak.
Transceiver (2-wire only)	10.	Monitor the non-grounded side of R55 with the scope. Increase the vertical sensitivity to 0.2 V/div.
Transceiver (2-wire only)	11.	Adjust R52 for a null in the tone. You are adjusting the line balance.
Transceiver	12.	Remove the RF tone from the transceiver.
Transceiver	13.	On the M9, monitor U13, pin 16 with the scope, dc coupled, 5 V/div.
Transceiver	14.	Adjust R7 so that the average voltage is 4 Vdc.
Control Head	15.	By pushing the buttons on the head, generate data pulses which must be made to trigger the scope once for each pulse.
Transceiver (M9RC PCB)	16.	Fine tune R7 if necessary so that there is an answer-back pulse coming from the M9 for each pulse generated at the control head.
Transceiver	17.	Display should say "RC ON" or "TC:XX." Monitor Q10 emitter with scope. Ground J6,3. Adjust R64 for 2.5 V peak-to-peak ac.

TABLE 12.1-1.
M9RC Remote Control Module, Test Procedure, Continued.

Control Head	18.	Generate data pulses by pressing buttons on the head and listen for the answer back pulses from the M9.
Transceiver	19.	Reconnect the RF tone into the receiver and verify that the data bursts are not affected.
Control Head	20.	Remove the RF tone.
Control Head	21.	Check transmit operation on all the normal transceiver test frequencies by entering them from channel "00".
Transceiver/Control Head	22.	A. Verify full power output on all test channels. B. Check RMT disable by removing accessory cable. Observe 0 to 1 Vdc on U13, 16.
Transceiver/Control	23.	Verify that the SC code can be entered from the head and check that the J2 outputs from M9 actually follow the programmed code. Use 170 and 85 for speed (170 = 10101010, 85 = 01010101).
Transceiver/Control Head	24.	Verify that the "UP" and "DN" functions operate and that the display on the head is keeping up with the transceiver.
Transceiver (M9RC PCB)	25.	Verify that the selective-call "SEND" feature works by: A. If there is a selcal in the unit, operate it and verify the RF output waveform on a scope. B. If no selcal is installed, place an ohmmeter across M9, J9 pins 4 and 5 and verify that the momentary short (about 100 ohms or so) is placed across these terminals by the circuit when the SEND button on the head is depressed.
Transceiver (M9RC PCB)	30.	Verify that the ATU feature works by pressing the button on the head and checking that there is a negative pulse output at M9, U22-6.
Transceiver (M9RC PCB)	31.	Verify the sideband select by monitoring the LSB and AM lines with a voltmeter and check transmit operation in both sidebands.
Transceiver (M9RC PCB)	32.	Verify that the "AMP ON/OFF" function works by connecting a small LED and resistor, or a small incandescent lamp across M9 J8 pin 6 and +12 V. With the "AMP" switch on the head in the ON position, when the transceiver is keyed, the lamp should go on, and with the switch on the OFF position, the lamp should never come on.
Control Head	33.	Check that the squelch operates.
Transceiver/Control Head	34.	Verify that the panel controls of the transceiver do not affect operation when in the remote mode. Check that the transceiver displays "R.C. OFF" when in remote mode. Check that the head displays "LOCAL" when in local mode. Verify that the panel controls of the radio operate normally by running through all functions as described in Section 4 (Operation).

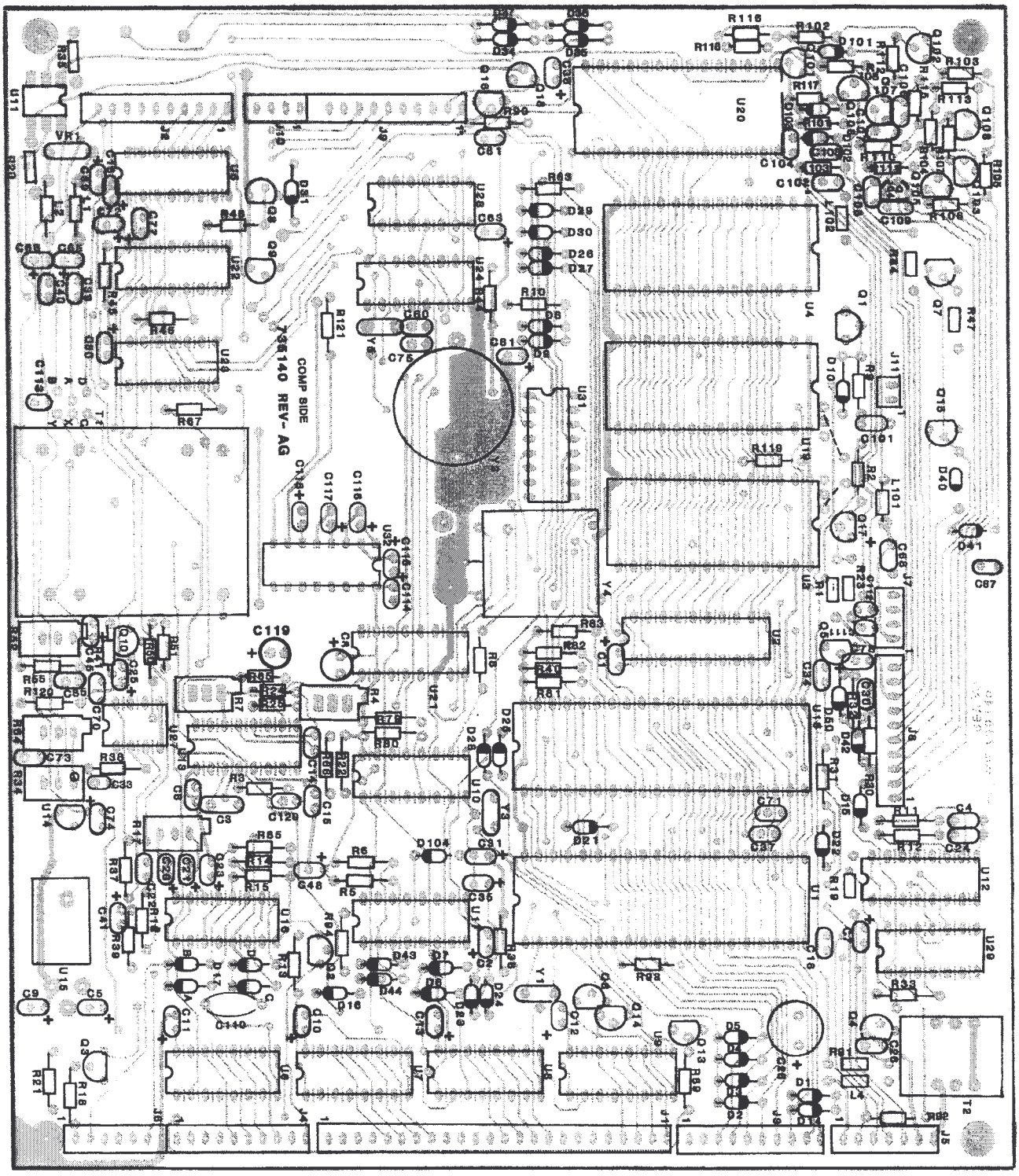
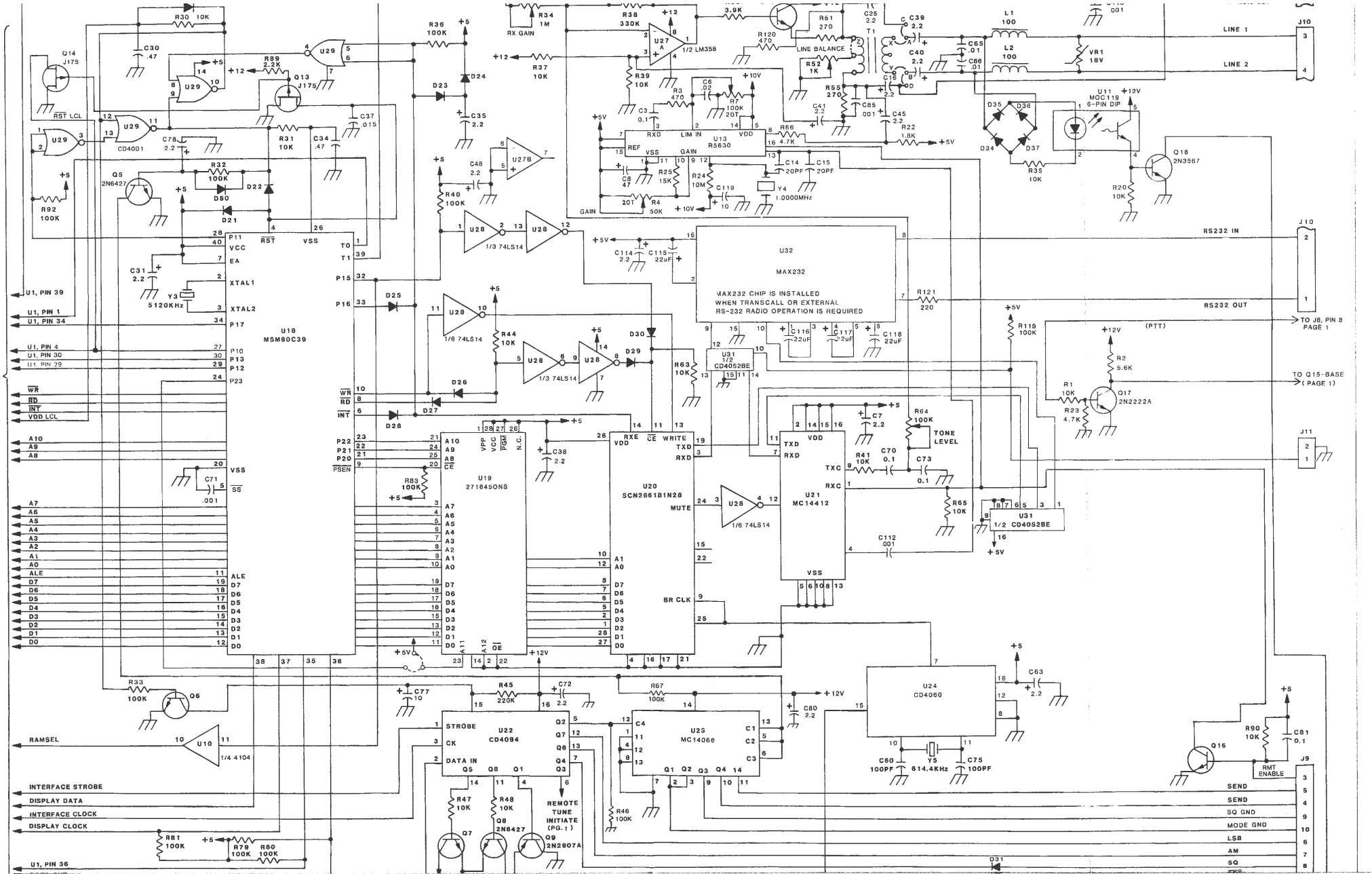
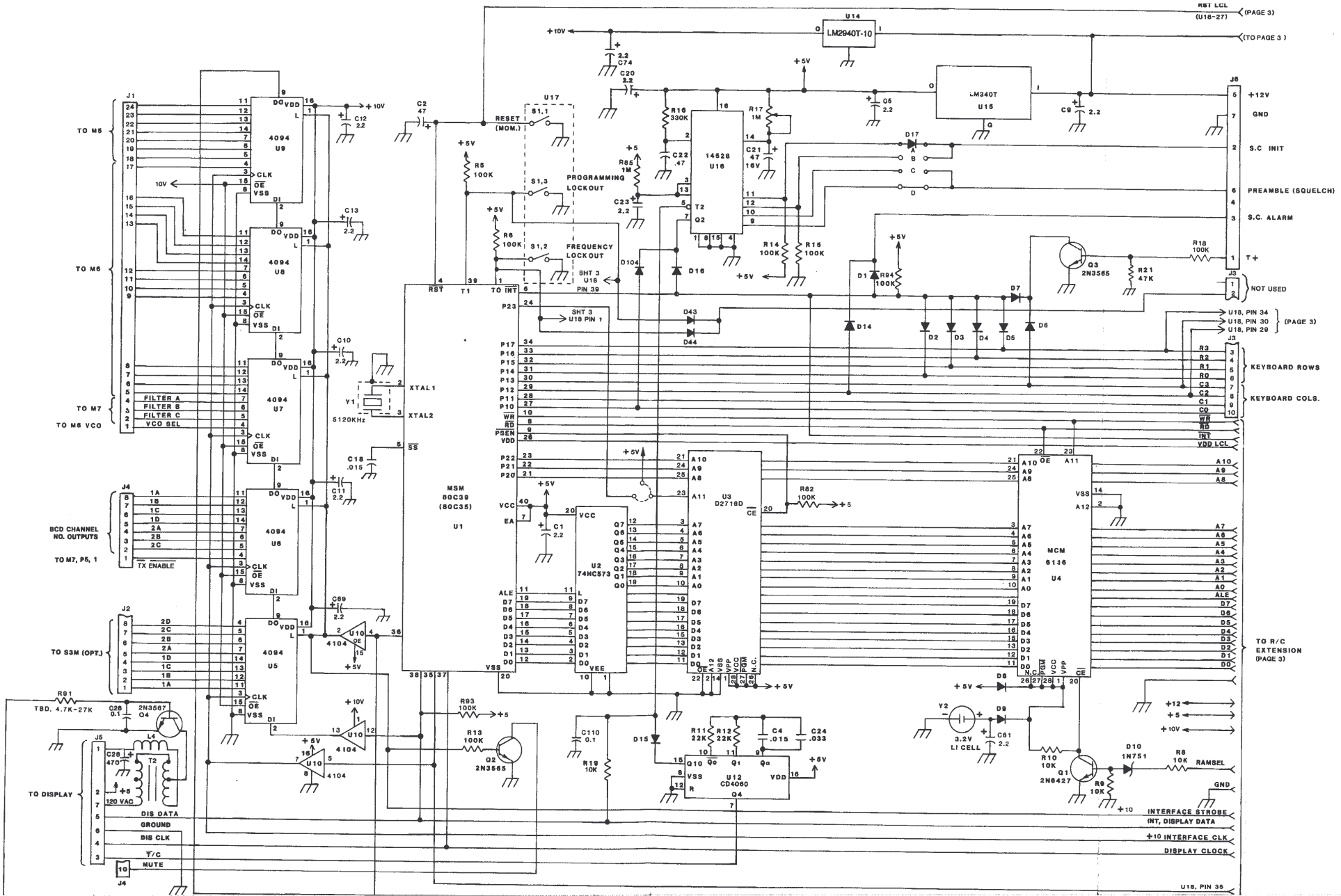


FIGURE 12.1-1.
Component Locations, Remote Control Module, M9RC.


U18
MSM80C39
U19
271645ONS
U20
SCN2661B1N28
U21
MC14412
U22
CD4094
U23
MC14066
U24
CD4060
U27
1/2 LM358
U13
R5630
U32
MAX232
MAX232 CHIP IS INSTALLED
WHEN TRANSCALL OR EXTERNAL
RS-232 RADIO OPERATION IS REQUIRED
U31
1/2 CD4052BE
U10
1/4 4104
U11
MOC119
6-PIN DIP
U28
1/6 74LS14
U28
1/3 74LS14
U29
CD4001
U27B
Y3
5120KHz
Y4
1.0000MHz
Y5
614.4KHz
LINE 1
LINE 2
LINE BALANCE
RS232 IN
RS232 OUT
TONE LEVEL
(PTT)
RX GAIN
GAIN
RAMSEL
RST LCL
VDD LCL
INTERFACE STROBE
DISPLAY DATA
INTERFACE CLOCK
DISPLAY CLOCK
REMOTE TUNE INITIATE (PG.1)
RMT ENABLE
SEND
SEND
SQ GND
MODE GND
LSB
AM
SQ
TO PAGE 2
TO J8, PIN 8 PAGE 1
TO Q15-BASE (PAGE 1)
U1, PIN 39
U1, PIN 1
U1, PIN 34
U1, PIN 4
U1, PIN 30
U1, PIN 29
U1, PIN 36


RST LCL (U18-27)
(PAGE 3)
(TO PAGE 3)
U14
LM2940T-10
+10V
+5V
LM340T U15
J6
+12V
GND
S.C INIT
PREAMBLE (SQUELCH)
S.C. ALARM
T+
J3
NOT USED
U18, PIN 34
U18, PIN 30
U18, PIN 29
(PAGE 3)
KEYBOARD ROWS
KEYBOARD COLS.
VDD LCL
TO M5
TO M6
TO M7
TO M6 VCO
FILTER A
FILTER B
FILTER C
VCO SEL
4094 U9
4094 U8
4094 U7
4094 U6
4094 U5
J1
J4
J2
BCD CHANNEL NO. OUTPUTS
TO M7, P5, 1
TX ENABLE
TO S3M (OPT.)
RESET (MOM.)
S1,1
S1,3
PROGRAMMING LOCKOUT
S1,2
FREQUENCY LOCKOUT
SHT 3 U18 PIN 39
SHT 3 U18 PIN 1
14528 U16
MSM 80C39 (80C35) U1
5120KHz
XTAL1
XTAL2
U3 D2716D
U2 74HC573
MCM 6136 U4
TO R/C EXTENSION (PAGE 3)
3.2V LI CELL
U12 CD4060
4104
2N3565
2N3567
2N6427
1N751
RAMSEL
GND
INTERFACE STROBE
INT, DISPLAY DATA
+10 INTERFACE CLK
DISPLAY CLOCK
TO DISPLAY
120 VAC
DIS DATA
GROUND
DIS CLK
T/C
MUTE
U16, PIN 35

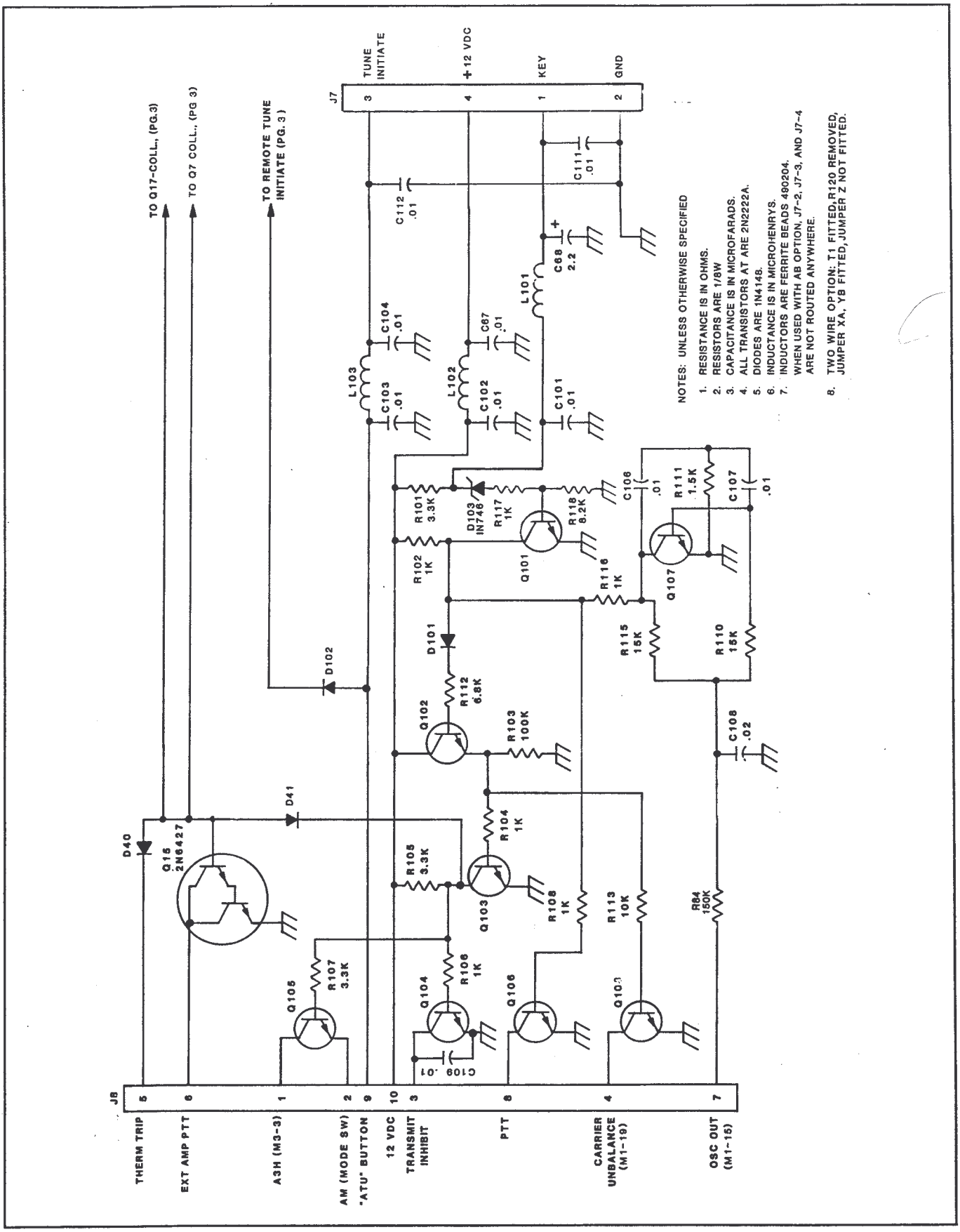


FIGURE 12.1-3.
Schematic Diagram, Antenna Tuner Interface.

TABLE 12.1-2.
Parts List, Remote Control Module, M9RC.

C1	241020	Capacitor, Tantalum 2.2 µF
C2	241047	Capacitor, Tantalum 35 V 0.47 µF
C3	275104	Capacitor, Monolithic 0.1 µF
C4	254153	Capacitor, Mylar 0.015 µF
C5	241020	Capacitor, Tantalum 2.2 µF
C6		Not Used.
C7	241020	Capacitor, Tantalum 2.2 µF
C8	231500	Capacitor, Electrolytic 16 V 47 µF
C9-C13	241020	Capacitor, Tantalum 2.2 µF
C14, C15	210200	Capacitor, Disc NPO 20 pF
C16	241020	Capacitor, Tantalum 2.2 µF
C17		Not Used.
C18	254153	Capacitor, Mylar 0.015 µF
C19		Not Used.
C20	241020	Capacitor, Tantalum 2.2 µF
C21	241476	Capacitor, Tantalum 47 µF
C22	241047	Capacitor, Tantalum 35 V 0.47 µF
C23	241020	Capacitor, Tantalum 2.2 µF
C24	254333	Capacitor, Mylar 0.033 µF
C25	241020	Capacitor, Tantalum 2.2 µF
C26	275104	Capacitor, Monolithic 50 V 0.1 µF
C27		Not Used.
C28	231471	Capacitor, Electrolytic 16 V 470 µF
C29		Not Used.
C30	241047	Capacitor, Tantalum 35 V 0.47 µF
C31	241020	Capacitor, Tantalum 2.2 µF
C32		Not Used.
C33	210100	Capacitor, Disc NPO 10 pF
C34	241047	Capacitor, Tantalum 35 V 0.47 µF
C35	241020	Capacitor, Tantalum 2.2 µF
C36		Not Used.
C37	254153	Capacitor, Mylar 0.015 µF
C38-C41	241020	Capacitor, Tantalum 2.2 µF
C42-C44		Not Used.
C45	275104	Capacitor, Monolithic 50 V 0.1 µF
C46,C47		Not Used.
C48	241020	Capacitor, Tantalum 2.2 µF
C49-C59		Not Used.
C60	210101	Capacitor, Disc NPO 100 pF
C61	241020	Capacitor, Tantalum 2.2 µF
C62		Not Used.
C63	241020	Capacitor, Tantalum 2.2 µF
C64		Not Used.
C65-C67	214103	Capacitor, Monolithic 50 V 0.01 µF
C68, C69	241020	Capacitor, Tantalum 2.2 µF
C70	275104	Capacitor, Monolithic 50 V 0.1 µF
C71	210102	Capacitor, Disc 0.001 µF
C72	241020	Capacitor, Tantalum 2.2 µF
C73	275104	Capacitor, Monolithic 50 V 0.1 µF
C74	241020	Capacitor, Tantalum 2.2 µF
C75	210101	Capacitor, Disc NPO 100 pF
C76		Not Used.
C77	231100	Capacitor, Electrolytic 16 V 10 µF
C78	241020	Capacitor, Tantalum 2.2 µF
C79		Not Used.

TABLE 12.1-2.
Parts List, Remote Control Module, M9RC, Continued.

C80	241020	Capacitor, Tantalum 2.2 μF
C81	275104	Capacitor, Monolithic 0.1 μF
C82-C84		Not Used.
C85	210102	Capacitor, Disc 0.001 μF
C86-C100*		Not Used.
C101*-C104*	214103	Capacitor, Monolithic 50 V 0.01 μF
C105*		Not Used.
C106*-C109*	214103	Capacitor, Monolithic 50 V 0.01 μF
C110	210104	Capacitor, Disc 25 V 0.1 μF
C111,C112	214103	Capacitor, Monolithic 50 V 0.01 μF
C113	210102	Capacitor, Disc 25 V 0.001 μF
C114	241020	Capacitor, Tantalum 2.2 μF
C115-C118	241226	Capacitor, Tantalum 22 μF
C119	237100	Capacitor, Tantalum 16 V 10 μF
D1-D9	320002	Diode, 1N4148
D10	320204	Diode, Zener 1N751
D11		Not Used.
D12-D16	320002	Diode, 1N4148
D17-D20		Not Used.
D21-D31	320002	Diode, 1N4148
D32,D33		Not Used.
D34-D37	320002	Diode, 1N4148
D38,D39		Not Used.
D40-D42	320002	Diode, 1N4148
D43-D49		Not Used.
D50	320002	Diode, 1N4148/1N4150
D51-D100		Not Used.
D101*, D102*	320002	Diode, 1N4148
D103*	320210	Diode, Zener 1N746
D104	320002	Diode, 1N4148
L1, L2	430014	Inductor, Molded Min 100 μH
L3		Not Used.
L4	430014	Inductor, Molded 100 μH
L5-L100		Not Used.
L101*-L103*	490204	Bead Ferrite
Q1	310064	Transistor, Darlington 2N6427
Q2, Q3	310006	Transistor, NPN 2N3565
Q4	310003	Transistor, NPN 2N3567
Q5	310064	Transistor, Darlington 2N6427
Q6, Q7	310006	Transistor, NPN 2N3565
Q8	310064	Transistor, Darlington 2N6427
Q9	310052	Transisitor, PNP PN2907A
Q10	310006	Transistor, NPN 2N3565
Q11,Q12		Not Used
Q13, Q14	310072	Transistor, J175
Q15	310064	Transistor, Darlington 2N6427
Q16	310006	Transistor, NPN 2N3565
Q17	310057	Transistor, NPN PN2222A
Q18	310003	Transistor, NPN 2N3567
Q19-Q100*		Not Used.
Q101*-Q108*	310057	Transistor, NPN PN2222A

TABLE 12.1-2.
Parts List, Remote Control Module, M9RC, Continued.

R1	113103	Resistor, Film 1/8 W 5% 10 kΩ
R2	113562	Resistor, Film 1/8 W 5% 5.6 kΩ
R3	113471	Resistor, Film 1/8 W 5% 470 Ω
R4	170205	Resistor, Trimmer 50 kΩ
R5,R6	113104	Resistor, Film 1/8 W 5% 100 kΩ
R7		Not Used.
R8-R10	113103	Resistor, Film 1/8 W 5% 10 kΩ
R11, R12	113223	Resistor, Film 1/8 W 5% 22 kΩ
R13-R15	113104	Resistor, Film 1/8 W 5% 100 kΩ
R16	113334	Resistor, Film 1/8 W 5% 330 kΩ
R17	170213	Resistor, Trimmer 1 MΩ
R18	113104	Resistor, Film 1/8 W 5% 100 kΩ
R19, R20	113103	Resistor, Film 1/8 W 5% 10 kΩ
R21	113473	Resistor, Film 1/8 W 5% 47 kΩ
R22	113182	Resistor, Film 1/8 W 5% 1.8 kΩ
R23	113472	Resistor, Film 1/8W 5% 4.7 kΩ
R24	113106	Resistor, Film 1/8 W 5% 10 MΩ
R25	113153	Resistor, Film 1/8 W 5% 15 kΩ
R26-R29		Not Used.
R30, R31	113103	Resistor, Film 1/8 W 5% 10 kΩ
R32, R33	113104	Resistor, Film 1/8 W 5% 100 kΩ
R34	170213	Resistor, Trimmer 1 MΩ
R35	113103	Resistor, Film 1/8 W 5% 10 kΩ
R36	113104	Resistor, Film 1/8 W 5% 100 kΩ
R37	113103	Resistor, Film 1/8 W 5% 10 kΩ
R38	113334	Resistor, Film 1/8 W 5% 330 kΩ
R39	113103	Resistor, Film 1/8 W 5% 10 kΩ
R40	113104	Resistor, Film 1/8 W 5% 100 kΩ
R41	113103	Resistor, Film 1/8 W 5% 10 kΩ
R42-R43		Not Used.
R44	113103	Resistor, Film 1/8 W 5% 10 kΩ
R45	113224	Resistor, Film 1/8 W 5% 220 kΩ
R46	113104	Resistor, Film 1/8 W 5% 100 kΩ
R47, R48	113103	Resistor, Film 1/8 W 5% 10 kΩ
R50	113392	Resistor, Film 1/8 W 5% 3.9 Ω
R51	113271	Resistor, Film 1/8 W 5% 270 Ω
R52	170209	Resistor, Trimmer 1 kΩ
R53-R54		Not Used.
R55	113271	Resistor, Film 1/8 W 5% 270 Ω
R56-R62		Not Used.
R63	113103	Resistor, Film 1/8 W 5% 10 kΩ
R64	170210	Resistor, Trimmer 100 kΩ
R65	113103	Resistor, Film 1/8 W 5% 10kΩ
R66	113472	Resistor, Film 1/8 W 5% 4.7 kΩ
R67	113104	Resistor, Film 1/8 W 5% 100 kΩ
R68-R78		Not Used.
R79-R83	113104	Resistor, Film 1/8 W 5% 100 kΩ
R84	113154	Resistor, Film 1/8 W 5% 150 kΩ
R85	113105	Resistor, Film 1/8 W 5% 1 MΩ
R86-R88		Not Used.
R89	113222	Resistor, Film 1/8 W 5% 2.2 kΩ
R90	113103	Resistor, Film 1/8 W 5% 10 kΩ
R91	TBD	Resistor, Film 1/8 W 5% 4.7 kΩ-27 kΩ
R92-R94	113104	Resistor, Film 1/8 W 5% 100 kΩ
R95-R100*		Not Used.

TABLE 12.1-2.
Parts List, Remote Control Module, M9RC, Continued.

R101*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R102*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R103*	113104	Resistor, Film 1/8 W 5% 100 kΩ
R104*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R105*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R106*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R107*	113332	Resistor, Film 1/8 W 5% 3.3 kΩ
R108*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R109*		Not Used.
R110*	113153	Resistor, Film 1/8 W 5% 15 kΩ
R111*	113152	Resistor, Film 1/8 W 5% 1.5 kΩ
R112*	113682	Resistor, Film 1/8 W 5% 6.8 kΩ
R113*	113103	Resistor, Film 1/8 W 5% 10 kΩ
R114*		Not Used.
R115*	113153	Resistor, Film 1/8 W 5% 15 kΩ
R116*, R117*	113102	Resistor, Film 1/8 W 5% 1 kΩ
R118*	113822	Resistor, Film 1/8 W 5% 8.2 kΩ
R119	113104	Resistor, Film 1/8 W 5% 100 kΩ
R120	113471	Resistor, Film 1/8 W 5% 470 Ω
R121	113221	Resistor, Film 1/8 W 5% 220 Ω
T1**	410028	Transformer, 600/600 Ohm Line
T2	410019	Transformer, 600/600 Ohm Line
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	IC, Programmed UPD2716D
U4	330149	IC, MCM6116P12 (120 ns)
U5-U9	330126	IC, CD4094BE/MC14094BCP
U10	330150	IC, F4104BPC
U11	320701	IC, MOC119
U12	330037	IC, CD 4060 BE
U13	330215	IC, RM5630AP
U14	330396	IC, LM2940T-10
U15	330076	IC, LM340T-5.0
U16	330115	IC, MC14528BCP
U17	530010	DIP Switch, 8 Sect SPST
U18	330142	IC, 80C39
U19	330102	IC, Programmed UPD2716D
U20	330167	IC, SCN2661BC1N28
U21	330180	IC, MC 14412VP
U22	330126	IC, CD4094BE/MC14094BCP
U23	330089	IC, MC14066
U24	330037	IC, CD 4060 BE
U25,U26		Not Used.
U27	330081	IC, LM348N
U28	330052	IC, SN74LS14N
U29	330054	IC, CD 4001B
U30		Not Used.
U31	330184	IC, CD4052BE
U32***	330315	IC, MAX232
VR1	350003	Varistor, 18 V
Y1	360018	Crystal, 5,120.000 kHz
Y2	750015	Battery, Lithium Button

TABLE 12.1-2.
Parts List, Remote Control Module, M9RC, Continued.

Y3	360018	Crystal, 5,120.000 kHz
Y4	360028	Crystal, 1.000MHz Microprocessor
Y5	363001	Resonator, Ceramic 614.4 kHz

* Indicates part located on automatic antenna tuner interface portion of PC board.
** Used for two-wire option.
*** Indicates part used only when TRANSCALL or external RS-232 option is installed.

12.2 SELCALL AND TRANSCALL OPTIONS

12.2.1 GENERAL

This section describes the operation and circuitry of the Selcall high-speed selective-calling system and the transcall automatic HF path evaluation and selective-calling system.

Section 12.2.3 covers the installation and operation of the Selcall option. Installation of the Transcall option is covered in Section 12.2.4 and Operation is detailed in Section 12.2.5. The technical circuit description for both the Selcall option and the Transcall option is described in Section 12.2.6.

12.2.1.1 SELCALL DESCRIPTION

The Selcall is a high-speed selective-calling system employing serial data communications capability via a built-in MODEM. The circuitry is contained on printed circuit boards 735152 and 735153 and mounted in a die-cast box over M3. Short call bursts are transmitted, followed by listening periods until contact is established. The unit is very reliable because the calling station may interrogate other stations repeatedly until a response is heard.

12.2.1.2 TRANSCALL DESCRIPTION

The Transcall is a path quality evaluation (PQE) system which allows the user to automatically select the best channel for communication with the station being called. Up to ten channels (1 through 10) may be scanned, although the optimum number seems to be five or six. The more channels that are scanned, the longer the system will take to acquire the called station.

The Transcall is contained in a standard die-cast box and is located over the M3 module. The 30-wire harness plugs into the module via two 15-pin subminiature "D" connectors. This option is a factory retrofit only. The PC board is identical with that of the Selcall, so that users who already have Selcall do not have to purchase an additional module.

The system operates by sending short interrogation bursts using a standard Bell 102 modem and 8-bit, 300-Baud serial data. Acknowledge request (ARQ) is used to assure the sending station that the call has been received. This is sometimes called a "handshake." By sending transmit code "000", all stations able to copy the call will sound their alarm tones and indicate "CALL" on their displays. This is the "ALL CALL" function. No handshake is issued in this case.

Experience has shown that the use of high-speed data transfers and the examination of a signal strength threshold is a very effective method for PQE. Further, since the modem is a period-counting device as opposed to an energy-detecting or PLL type, it handles multipath very well. Only when conditions are severe will the system reject the channel with the multipath, even if the signal is strong.

To make its evaluations, the called station transmits 32 characters on each of the available channels. The other station tries to copy these characters, and gives each channel a score based on correct copy. If a character is received correctly, that channel is given one point. If the signal strength on that channel is over the preset threshold (see below) when the character was copied correctly, that channel is given another point. Therefore, the maximum score is 64. The system picks the channel with the highest score. In the case of a tie, the system will pick channels according to the following:

1. If the highest channel number in the scan is one of the ones involved in the tie, it will be selected. I.e., if scanning 6 channels and channel 6 is in the tie, channel 6 will be selected.

2. Otherwise, the lowest channel number will be selected.

12.2.2 SPECIFICATIONS

Table 12.2-1 lists the specifications for the Selcall option. Table 12.2-2 lists the specifications for the Transcall option.

12.2.3 SELCALL INSTALLATION AND OPERATION

12.2.3.1 RECEIVE CODE

Each unit in the system should be assigned a different receive code. Units are preset before shipment and the code is marked on the outside of the transceiver. If it is desired that all transceivers in a system be factory preset, it should be so indicated on the sales order. If it is desired to change the preset receive code, remove the top cover of the transceiver, and remove the option module cover.

Set the code on the eight-position DIP switch, S2, located in the middle of the circuit board. Refer to Table 12.2-3 to match the programmed receive code with its corresponding decimal transmit code.

12.2.3.2 TRANSMIT CODE

The transmitted code is set using the keypad and the method outlined in the transceiver manual. The three-digit decimal number which is entered corresponds to the complement of the receive code.

12.2.3.3 INITIATING CONTACT

Complete operating instructions will be found in Section 4, but it is as simple as pressing the "S.C." button on the transceiver panel, entering the 3-digit decimal code of the station to be called, and pressing the "CALL" button. If the station receives the call correctly, a transpond signal of about 2 seconds duration will be sent immediately after the calling station's transmitter has stopped. The clarifier must be "OFF" for Selcall use.

TABLE 12.2-1.
Selcall Specifications.

SUPPLY VOLTAGE:	12 Vdc nominal.
SUPPLY CURRENT:	150 mA average.
DATA RATE:	300 Baud.
DATA FORMAT:	8-bit, 1 stop, no parity.
MARK FREQUENCY:	2250 Hz.
SPACE FREQUENCY:	2050 Hz.
CALL BURST LENGTH:	About 200 ms.
LISTENING INTERVAL:	About 400 ms.
ACKNOWLEDGE LENGTH:	About 2 seconds.
TONE FREQUENCY TOLERANCE:	±30 Hz.
NUMBER OF POSSIBLE CODES:	255.
ALL-CALL CODE:	000.
CONTROLS:	"CALL" button; press once to send, again to stop.

TABLE 12.2-2.
Transcall Specifications.

SUPPLY VOLTAGE:	12 Vdc nominal.
SUPPLY CURRENT:	150 mA average.
DATA RATE:	300 Baud.
DATA FORMAT:	8-bit, 1 stop, no parity.
MARK FREQUENCY:	2250 Hz.
SPACE FREQUENCY:	2050 Hz.
TONE FREQUENCY TOLERANCE:	±30 Hz.
NUMBER OF POSSIBLE CODES:	255.
ALL-CALL CODE:	000.
ACQUISITION TIME:	300 seconds max.* 180 seconds typ. (not in sync).* 15 seconds typ. (in sync).*
TOTAL ADDITIONAL TIME:	60 seconds max. (after initial acquisition).* 30 seconds typ. (after initial acquisition).*
CONTROLS:	"CALL" button, press once to send, again to stop. "SCAN LIMIT" switch, set positions 1-4 of S1 (Selcall) to BCD representation of selected scan limit. (Switch 1 of S1=MSB, "ON"=1, 10 channels max.) "MODE" switch functions are as follows:

SELECTION	FUNCTIONS
T.C.	TRANSCALL on only.
S.C.	SELCALL on, radio functions normally.

*Based on 10-channel scan.

12.2.4 TRANSCALL INSTALLATION

12.2.4.1 RECEIVE CODE

Each unit in the system should be assigned a different receive code. Units are preset before shipment and the code is marked on the outside of the transceiver. If it is desired that all transceivers in a system be factory preset, it should be so indicated on the sales order. If it is desired to change the preset receive code, remove the top cover of the transceiver, and remove the option module cover. Set the code on the eight-position DIP switch, S2, located in the middle of the circuit board. Refer to Table 12.2-3 to match the programmed receive code with its corresponding decimal transmit code.

12.2.4.2 TRANSMIT CODE

The transmitted code is set using the keypad and the method outlined in Section 4 of this manual.

The three-digit decimal number which is entered corresponds to the complement of the receive code.

12.2.4.3 SCAN LIMIT

The scan-limit switch allows the user to set the number of channels that are to be scanned. Transcall scans only the first ten channels, starting with the current channel. The scan advances up to the scan limit, then repeats starting on channel 1. Valid scan-limit codes range from 2 to 10. Each unit in the system should be assigned the same scan limit code for proper operation. The operator should set his most preferred channels in the lower channel numbers to ensure that the best channel is selected during the path evaluation sequence. To change the scan-limit code, remove the top cover of the transceiver, and remove the option module cover. Set the code on positions 1-4 of the eight-position DIP switch, S1, located in the middle of the circuit board. Refer to Table 12.2-4 to set the switch to the desired scan limit.

12.2.4.4 SIGNAL-STRENGTH THRESHOLD

The signal-strength threshold is preset by the factory, but can be set by the user for more accurate path evaluations. To change the signal-strength threshold, remove the top cover of the transceiver, and remove the option module cover. Adjust R30 as indicated by Table 12.2-5.

12.2.5 TRANSCALL OPERATION

12.2.5.1 OPERATION

The Transcall operates and the unit scans under the control of the Transcall when the panel switch is in the "TC" (Transcall ON) position. In the "SC" (Selcall ON) position, the Transcall will neither send nor receive any Transcall interrogations, but operates as a normal Selcall. In this position, the normal scan mode of the transceiver may be used by pressing "SCAN" (see Section 4 of this manual).

When the Transcall is ON, the panel keypad is disabled and the user may not select channels, frequencies, or change the transmitted S.C. code. To regain panel control, first turn the panel switch AWAY from the "TC" position to the "SC" position. Then press the "F" button on the panel. A couple of seconds later, the display should change from "t.c." to the normal "CH: ". This indicates that panel control is now available. This must be done to change the transmitted code. To restart the Transcall scan, turn the switch back to the "TC" position.

Turning Transcall off for at least 3 seconds resets the scan delay. The scan delay is started after a successful calling sequence or after PTT and lasts 60 seconds.

12.2.5.2 INITIATING TRANSCALL

Operating Transcall is as simple as entering the code of the station to be called (as described previously), setting the MODE switch to "TC" and finally pressing the "CALL" button. Transcall will assume control of the transceiver to find the channel that has the best path conditions between the originating and remote stations.

12.2.5.3 TRANSCALL SCAN

When setting the MODE switch to "TC", the transceiver switches to Transcall operation and initiates Transcall scanning. This is indicated on the LCD display which shows the characters "tc : XX", where "XX" is the current channel number. The Transcall scan sequence begins on the current channel, advances and continues up to the scan limit. As the scan reaches the limit, it begins again starting on channel 1. Transcall monitors the current channel of the scan sequence for three seconds, listening for any valid selective-call or Transcall transmissions.

12.2.5.4 INITIATING CONTACT

After pressing the "CALL" button, an "arming tone" will sound through the loudspeaker to indicate that the pressing of the key was recognized. Transcall will then call the desired remote station in an attempt to sync its scan sequence to step with the originating station in real time.

The operator may begin calling on the channel of his choice by pressing the "CALL" button when the channel prior to the desired channel is reached in the scan sequence. Synchronization between stations can also be attained by powering up both transceivers (with the mode switch of both units set to "TC") at the same time.

After "CALL" is pressed and the channel changes to the next channel in the sequence, Transcall will then send an attention burst to the remote station for a period of 200 ms. During that period, the push-to-talk (PTT) relay switches on, the proper harmonic filter is set and then the attention burst is sent. Transcall will then switch to receive (which switches the PTT relay off) and listen for the acknowledge for a period of 400 ms. Transcall calls on each channel initially for three seconds and completes three send-listen cycles during that period. The send-listen cycle can be identified by the clicking of the relays as they switch between the send and receive mode. The calling

TABLE 12.2-3.
Selective-Call Conversion Chart.

TX CODE	RX SWITCHES ON	TX CODE	RX SWITCHES ON
001	2345678	053	2 4 78
002	1 345678	054	1 4 78
003	345678	055	4 78
004	12 45678	056	123 78
005	2 45678	057	23 78
006	1 45678	058	1 3 78
007	45678	059	3 78
008	123 5678	060	12 78
009	23 5678	061	2 78
010	1 3 5678	062	1 78
011	3 5678	063	78
012	12 5678	064	123456 8
013	2 5678	065	23456 8
014	1 5678	066	1 3456 8
015	5678	067	3456 8
016	1234 678	068	12 456 8
017	234 678	069	2 456 8
018	1 34 678	070	1 456 8
019	34 678	071	456 8
020	12 4 678	072	123 56 8
021	2 4 678	073	23 56 8
022	1 4 678	074	1 3 56 8
023	4 678	075	3 56 8
024	123 678	076	12 56 8
025	23 678	077	2 56 8
026	1 3 678	078	1 56 8
027	3 678	079	56 8
028	12 678	080	1234 6 8
029	2 678	081	234 6 8
030	1 678	082	1 34 6 8
031	678	083	34 6 8
032	12345 78	084	12 4 6 8
033	2345 78	085	2 4 6 8
034	1 345 78	086	1 4 6 8
035	345 78	087	4 6 8
036	12 45 78	088	123 6 8
037	2 45 78	089	23 6 8
038	1 45 78	090	1 3 6 8
039	45 78	091	3 6 8
040	123 5 78	092	12 6 8
041	23 5 78	093	2 6 8
042	1 3 5 78	094	1 6 8
043	3 5 78	095	6 8
044	12 5 78	096	12345 8
045	2 5 78	097	2345 8
046	1 5 78	098	1 345 8
047	5 78	099	345 8
048	1234 78	100	12 45 8
049	234 78	101	2 45 8
050	1 34 78	102	1 45 8
051	34 78	103	45 8
052	12 4 78	104	123 5 8

TABLE 12.2-3.
Selective-Call Conversion Chart, Continued.

TX CODE	RX SWITCHES ON	TX CODE	RX SWITCHES ON
105	23 5 8	156	12 67
106	1 3 5 8	157	2 67
107	3 5 8	158	1 67
108	12 5 8	159	67
109	2 5 8	160	12345 7
110	1 5 8	161	2345 7
111	5 8	162	1 345 7
112	1234 8	163	345 7
113	234 8	164	12 45 7
114	1 34 8	165	2 45 7
115	34 8	166	1 45 7
116	12 4 8	167	45 7
117	2 4 8	168	123 5 7
118	1 4 8	169	23 5 7
119	4 8	170	1 3 5 7
120	123 8	171	3 5 7
121	23 8	172	12 5 7
122	1 3 8	173	2 5 7
123	3 8	174	1 5 7
124	12 8	175	5 7
125	2 8	176	1234 7
126	1 8	177	234 7
127	8	178	1 34 7
128	1234567	179	34 7
129	234567	180	12 4 7
130	1 34567	181	2 4 7
131	34567	182	1 4 7
132	12 4567	183	4 7
133	2 4567	184	123 7
134	1 4567	185	23 7
135	4567	186	1 3 7
136	123 567	187	3 7
137	23 567	188	12 7
138	1 3 567	189	2 7
139	3 567	190	1 7
140	12 567	191	7
141	2 567	192	123456
142	1 567	193	23456
143	567	194	1 3456
144	1234 67	195	3456
145	234 67	196	12 456
146	1 34 67	197	2 456
147	34 67	198	1 456
148	12 4 67	199	456
149	2 4 67	200	123 56
150	1 4 67	201	23 56
151	4 67	202	1 3 56
152	123 67	203	3 56
153	23 67	204	12 56
154	1 3 67	205	2 56
155	3 67	206	1 56

TABLE 12.2-3.
Selective-Call Conversion Chart, Continued.

TX CODE	RX SWITCHES ON	TX CODE	RX SWITCHES ON
207	56	232	123 5
208	1234 6	233	23 5
209	234 6	234	1 3 5
210	1 34 6	235	3 5
211	34 6	236	12 5
212	12 4 6	237	2 5
213	2 4 6	238	1 5
214	1 4 6	239	5
215	4 6	240	1234
216	123 6	241	234
217	23 6	242	1 34
218	1 3 6	243	34
219	3 6	244	12 4
220	12 6	245	2 4
221	2 6	246	1 4
222	1 6	247	4
223	6	248	123
224	12345	249	23
225	2345	250	1 3
226	1 345	251	3
227	345	252	12
228	12 45	253	2
229	2 45	254	1
230	1 45	255	
231	45		

TABLE 12.2-4.
Scan Limits.

No. of Channels Scanned	Set SW1 Segs On
3	2
4	4 2
5	32
6	432
7	1
8	4 1
9	3 1
10	43 1

TABLE 12.2-5.
Signal-Strength Threshold Settings.

SINAD	SIGNAL	AGC (VDC)
9.5	-121 (0.2 μV)	4.04
25	-98 (2.82 μV)	4.02
	-97	3.81
	-96	3.45
	-95	3.16
	-94	2.95
	-93	2.81
	-92	2.69
	-91	2.62
	-90	2.55
	-88	2.45
	-86	2.37
	-84	2.31
	-82	2.24
	-80 (22.4 μV)	2.19
	-75	2.05
	-70 (70 μV)	1.91
	-65	1.76
	-60	1.60
	-55	1.44
	-50 (700 μV)	1.27
	-45 (1.26 mV)	1.10
	-35 (4 mV)	0.769
	-25 (12.6 mV)	0.477

station continues to call on each channel of the scan sequence until all channels have been tried.

If the path conditions are poor or the scan sequence of the remote is greatly out of step, contact may not be made after the initial acquisition sequence. In that case, the sequence will repeat, this time calling each channel in the sequence for a period equal to (scan limit x 4) + 4 seconds. This gives the station being called time to scan across the calling channel. If no contact is made after the previous sequence, an audible "no-contact" signal is issued.

12.2.5.5 PATH QUALITY EVALUATION

When the remote station responds, a string of 32 packets containing the number AA hexadecimal is sent back to acknowledge contact. Both stations, which are now in sync, step to the next channel and attempt contact until all the channels in the sequence have been tried. The remote station will not attempt contact on channels which exceed the preset signal strength threshold level indicating that the channel is already busy. After all channels have been tried, the remote station continues scanning while the originating station stops its scan to evaluate the path conditions.

The bit error rate (BER) of the answer-back packets from each channel are counted and stored in memory. The BER gives an indication of the propagation conditions between the stations. The signal strength level of the received signal is checked and this information is stored for each channel. Transcall then evaluates the BER and signal strength data and selects the channel that represents the best path between the two stations. It then sends the basic selective-call bursts on the selected channel, waiting for the remote station to scan to the channel and send its acknowledge. When the acknowledge is received, the "call alarm" tone will sound at both stations to inform the operator that the best channel has been selected and the call message will be displayed at the remote station. The path evaluation sequence is completed and both stations are now set to the channel which has the best path between them.

During poor signal conditions, the remote station may not respond to the initial selective call that identifies the best channel. In that case, the originating station will keep sending selective call bursts for about 90 seconds to give the remote station a good chance to respond. If no contact is made at all after that period, a "no contact" beeping tone will be heard at the sending station and both stations will then resume (Transcall) scanning.

After the "call alarm" tone is issued, both stations will stay on the selected channel for 60 seconds. Both stations will

resume scanning at the same time, which maintains the sync of the scan sequences.

12.2.6 SELCALL AND TRANSCALL TECHNICAL CIRCUIT DESCRIPTION

12.2.6.1 CIRCUIT DESCRIPTION

The Transcall/Selcall circuit is based on the 80C39 microprocessor (U1), which is a 40-pin IC having 27 input/output lines used fo communication with the rest of the circuitry. Shown below is a description of the 80C39 processor indicating pinouts and line names.

Pin No.	Name	Description
1	T0	Test 0; One-bit I/O port
2	XTAL 1	5.120 MHz Ref. Osc.
3	XTAL 2	5.120 MHz Ref. Osc.
4	$\overline{\text{RESET}}$	Reset; initializes the CPU
5	$\overline{\text{SS}}$	Single-step; tied to reset
6	$\overline{\text{INT}}$	Interrupt; connected to "SEND" switch and UART RX data line
7	$\overline{\text{EA}}$	ROM Mode; +5 Vdc
8	$\overline{\text{RD}}$	Read; GRD to read external memory
9	$\overline{\text{PSEN}}$	Program Store Enable; GRD to fetch instruction from external memory
10	$\overline{\text{WR}}$	Write; GRD to write to external memory
11	ALE	Address clock; to external memory
12	DB0	Data Bus Port
13	DB1	Data Bus Port
14	DB2	Data Bus Port
15	DB3	Data Bus Port
16	DB4	Data Bus Port
17	DB5	Data Bus Port
18	DB6	Data Bus Port
19	DB7	Data Bus Port
20	V_{SS}	Ground
21	P20	I/O Port # 2
22	P21	I/O Port # 2
23	P22	I/O Port # 2
24	P23	I/O Port # 2
25	PROG	N/A
26	V_{DD}	+5 Vdc
27	P10	I/O Port # 1
28	P11	I/O Port # 1
29	P12	I/O Port # 1
30	P13	I/O Port # 1
31	P14	I/O Port # 1
32	P15	I/O Port # 1
33	P16	I/O Port # 1
34	P17	I/O Port # 1
35	P24	I/O Port # 2
36	P25	I/O Port # 2
37	P26	I/O Port # 2
38	P27	I/O Port # 2
39	T1	Test 1; One-bit I/O port
40	V_{CC}	+5 Vdc

12.2.6.2 PORT LINES

Data Bus Port

One of the eight-bit ports is called the bus port and performs a dual function in the system. First it acts as a port for the other devices on the bus; these include the read-only memory (ROM), U3, and the universal asynchronous receiver/transmitter (UART), U4. Second, the data bus is time multiplexed with the lower eight bits of the internal program counter such that the external latch, U2, latches those address bits at the proper time in conjunction with the address latch enable signal (ALE). The data bus port is located at U1 pins 12 through 19, and ALE is pin 11.

I/O Port # 1

This input/output port is split up among various system communications requirements.

P11 An optional input providing AGC data to the processor. It is connected via D9 to the output (pin 14) of U13. During the alignment procedure, variable resistor R30 is adjusted so that its wiper reads 2.1 volts. When the receive signal strength exceeds a certain threshold, U13-pin 14 goes from HI to LO, which pulls P11 to ground.

P12 An input which is normally LO and goes HI when the TC/SC switch is put in the Transcall position.

P13 An output hooked to open collective transistor Q6. This line is used to enable the "MUTE" function in the transceiver when the SC/TC switch is in the Selcall position.

P14 An input which normally provides AGC data to the processor via U13 pin 7. Hooked in parallel with the optional AGC circuit feeding P11, it has a different time constant.

P15 An output providing RS232 data to the main processor in the transceiver.

P16 An input accepting RS232 data from the main processor. It is also tied via D5 to the reset (pin 4) and single step (pin 5) processor inputs.

P17 An output alarm tone which is tied to the CW sidetone line going to the M1 audio module.

I/O Port # 2

This input/output port is also split up among various system communication requirements.

P20 Most significant address line to U3.

P21 Second most significant address line to U3.

P22 Third most significant address line to U3.

P23 An input tied to the transceiver PTT line.

P24 An output providing clock data via U13 to U15, U10, U9 and U8.

P25 An output providing strobe data via U13 to U15, U10, U9 and U8.

P26 An output via inverter U11B to Q1. It is used to activate the PTT line when required during the Selcall or Transcall modes.

P27 An output via inverter U11A to Q2. It is used to activate the Selcall alarm controlled by the main processor.

Miscellaneous Ports

XTAL1, XTAL2 The crystal at Y3 provides the clock for the CPU. This crystal must be trimmed by C25 to provide proper synchronization between radios.

T0 An input from the SC/TC switch. +5 Vdc in Selcall position, ground in Transcall.

T1 An input from shift register U8. It allows the processor to read the Selcall code data when it is being shifted in.

12.2.6.3 UART

The IC U4 is the UART. It provides the serial interface to and from the CPU. Serial information is received from the modem, U5, via the RXD line pin 3. Upon receipt of a valid character, the UART sends an interrupt to the CPU via the RXE line, pin 14. Data is passed to the CPU when the CE line, pin 11, is low and the WRITE line, pin 13, is high.

Data is sent to the UART from the CPU when CE and WRITE are low. Serial data from the UART is passed to the modem on the TXD line, pin 19. During transmission of serial data to the modem pin 24 of the UART will be low. This controls the mute line on the modem and turns on the modem tone. U7 provides the baud rate clock for the UART. This clock is derived from a 614.4-kHz ceramic resonator.

12.2.6.4 MODEM/FILTER/LEVEL AMP

The modem, filter, and level amplifier are made up of U5, U6, Q4 and Q5 respectively. Receive audio enters U6 on pin 8. This signal is amplified in an internal op amp whose gain is set by the values of resistors R18 and R19. The output of the op amp is fed internally to the filter section whose output appears at pin 3. This filter output is then coupled via the capacitor on pin 3 through R16 to the comparator input on pin 2. R15 provides an adjustment to allow the output of the comparator to be set to a square wave at pin 16. The crystal at Y1 provides the clock required by the filter and the modem. Output of U6 is taken from pin 16 and applied to the RXC input, pin 1 of U5, the modem. The modem takes the frequency shift data and converts it into a TTL level digital signal the UART can use. In transmit the serial data is taken from the UART on pin 19 and enters the modem on U5 pin 11. The high on the mute line, pin 12 enables the output tone on the TXC line, pin 9. As data is shifted in on pin 11 the output tone is shifted between the two FSK frequencies. Output from U5 pin 9 enters the level amplifier through C9 and the level adjust pot R21. The resistors R25 and R24 set the gain of Q4 to approximately 15. Q5 is an emitter follower to provide buffering to Q4.

12.2.6.5 CPU CONTROL-CODE INPUT

Control codes for the Selcall such as scan limits, channel information, transmit code, and receive code are presented to the CPU in a serial data format. U8, U9, U10, and U15 are parallel-in serial-out shift registers. A high on the strobe input, pin 9 for at least one rising edge of the clock input, pin 10 latches the data on the parallel input lines. Releasing the strobe line and toggling the clock line causes data to be shifted out pin 3 on the rising edge of the clock. The four shift registers are connected in series with U8 being closest to the CPU. Scan limits are set as a binary number on the first four lines of S1.

The receive code is set on S2. The transmit code and the channel information is input to U10 and U15 as parallel information coming from the M9 module.

The CPU directly controls the reading of these shift registers through the use of port 2 lines P24 and P25.

U13 performs the necessary level shifting to interface the TTL levels provided by the CPU to the 8.7-V levels needed by the shift registers. P25 becomes the strobe signal for the shift registers and P24 is the clock signal. The CPU can access the data it requires by issuing the proper number of clock "ticks". Shift register data is read by the CPU test pin T1, pin 39.

TABLE 12.2-6.
Test Procedure.

1. Make a visual inspection of the Selcall or Transcall module for any missing or wrong components, solder bridges, incorrect wiring, etc.

2. Make an ohm check from the +12 line to ground at U14, the +5 line at U14, and the +8.7 line at U12. The readings should show several hundred ohms.

3. Connect the module to the harness on top of M3 of the TW100 transceiver. Connect the transceiver to its power supply and power up.

4. Adjust C26 so that the frequency at pin 11 of the CPU (ALE) is close to 341.333 kHz as possible.

5. Remove U11. Adjust R21 (tone level) so that the voltage at the emitter of Q5 is approximately 0.5 Vac P-P. Replace U11.

6. Adjust R15 so that the waveform at pin 16 of U6 is clipping at 0 V and 5 V (hitting the rails). No RF receiver input should be applied.

7. Set R30 so that the wiper of R30 reads 2.1 V. Use FET input meter or oscilloscope.

8. Verify that each input bit of U8 and U9 toggles when the corresponding switch of U8, U9 is toggled. (Refer to schematic).

9. Check that the signals $\overline{INT}$, $\overline{WR}$, $\overline{PSEN}$, and ALE are at correct TTL levels.

10. Measure the risetime of the clock signal at pin 10 of U10. Verify that it is no greater than 15 microseconds from 0 V to 8 V.

11. Verify that the frequency at U7, pin 5 reads 19.2 kHz.

12. Verify the operation of the SELCALL/TRANSCALL module.

Receiving a call:

A. Connect a load (12 V-lamp or etc.) to the collector of Q3 (refer to schematic). Install the Selcall module with SELCALL software in U3.

B. Using a transceiver with a working SELCALL installed, operate it sending to the unit under test. Make sure that the receive code of the unit under test is set to the same code of the sending transceiver.

C. When a proper call is received, the "CALL: _____" prompt should be displayed and the "ring" tone should be heard. Verify that the load (of step A) is switched on also.

Initiating a call:

A. Send using the transceiver with the unit under test and verify that it functions correctly.

13. Verify that the RF output power is 100 W when the SELCALL is sending.

TABLE 12.2-7.
Transcall Final Test Procedure.

1. Make sure that each transceiver and Selcall module has been tested and aligned properly.
2. Set the scan limit switch (refer to Table 12.2-4) of both transceivers to scan 6 channels.
3. Set one transceiver's receive code to 170 and its transmit code to 85. Set the other transceiver's receive code to 85 and its transmit code to 170 (refer to Table 12.2-3).
4. Connect both transceivers as illustrated in Figure 12.2-1.
5. Set the mode switch of both units to "SQUELCH ON" and power up both units.
6. While enabling the PTT, speak into the microphone and adjust the attenuator so that the signal strength barely moves off of zero. Check this in the other direction also.
7. Check the Transcall scan. Switch the mode of one unit to "TC" and check that the transceiver is scanning (as indicated on the LCD display). Make sure that it scans to channel 6 and then repeats on channel 1. Verify this also on the other transceiver.
8. Check the Transcall PQE operation. Press the "CALL" button of one transceiver (which is now the originating station). Verify that the transceiver sends on each channel until it receives the acknowledge from the other unit.
9. After the transceiver receives the answer back, verify that the other unit (remote station) syncs its scan with the originating station. Verify that the remote station sends the PQE burst on each channel, until all channels have been tried.
10. The originating station will decide which channel has the best path quality and then will send selcall bursts on that channel. Verify that the remote station scans around to the selected channel and that the "ring" signal sounds at both stations.
11. Verify that the "CALL: xx" message is also displayed at the called station. Check that both stations stay on the selected channel for 60 seconds before they resume scanning.
12. Repeat steps 8 through 11 in the other direction.

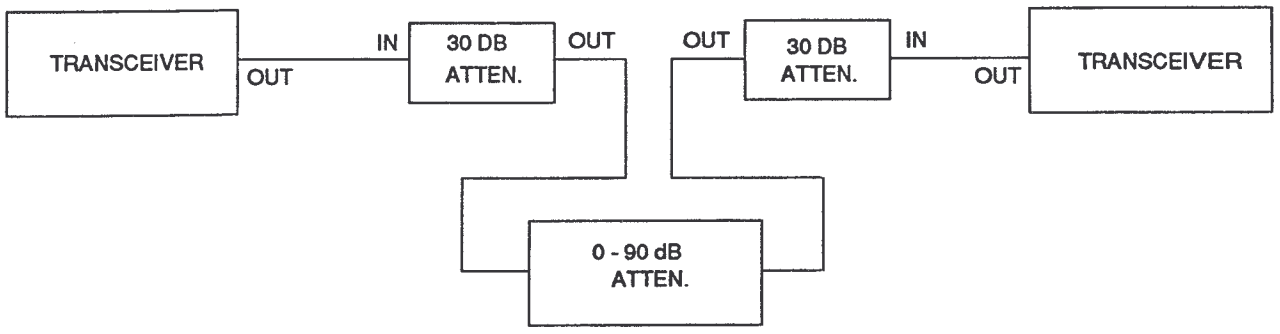
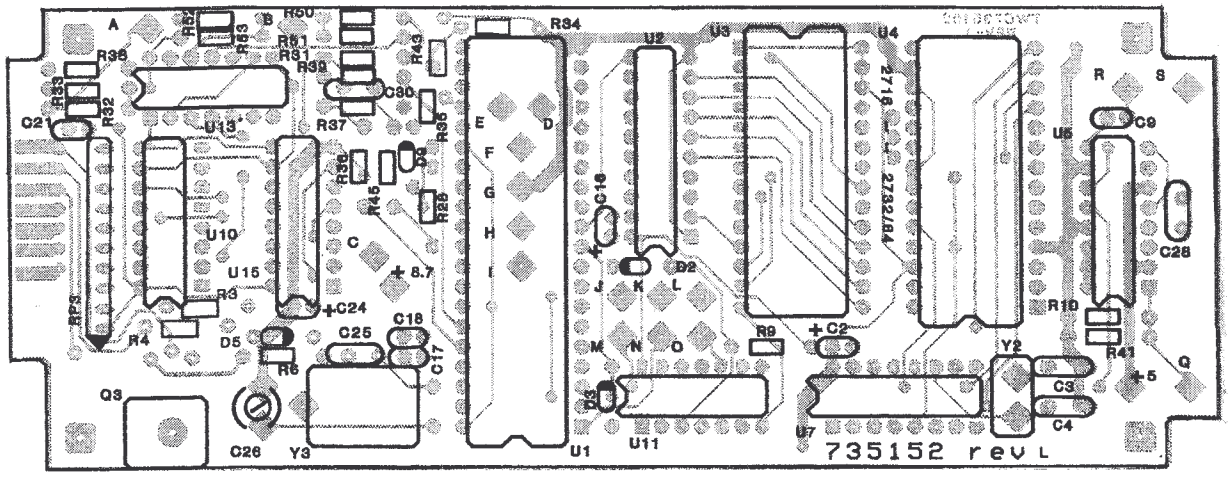


FIGURE 12.2-1.
Transceiver Connections.



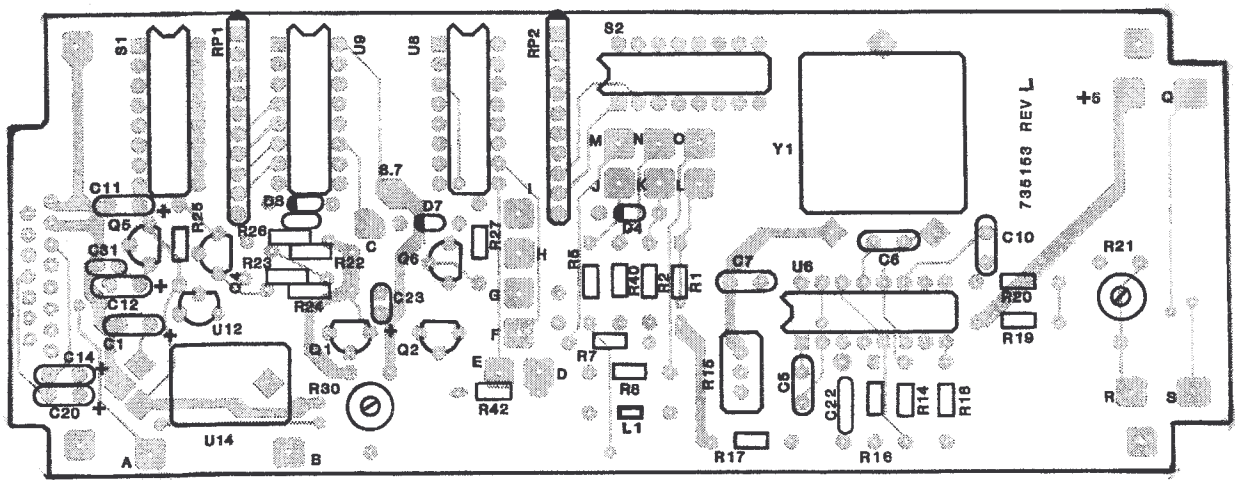
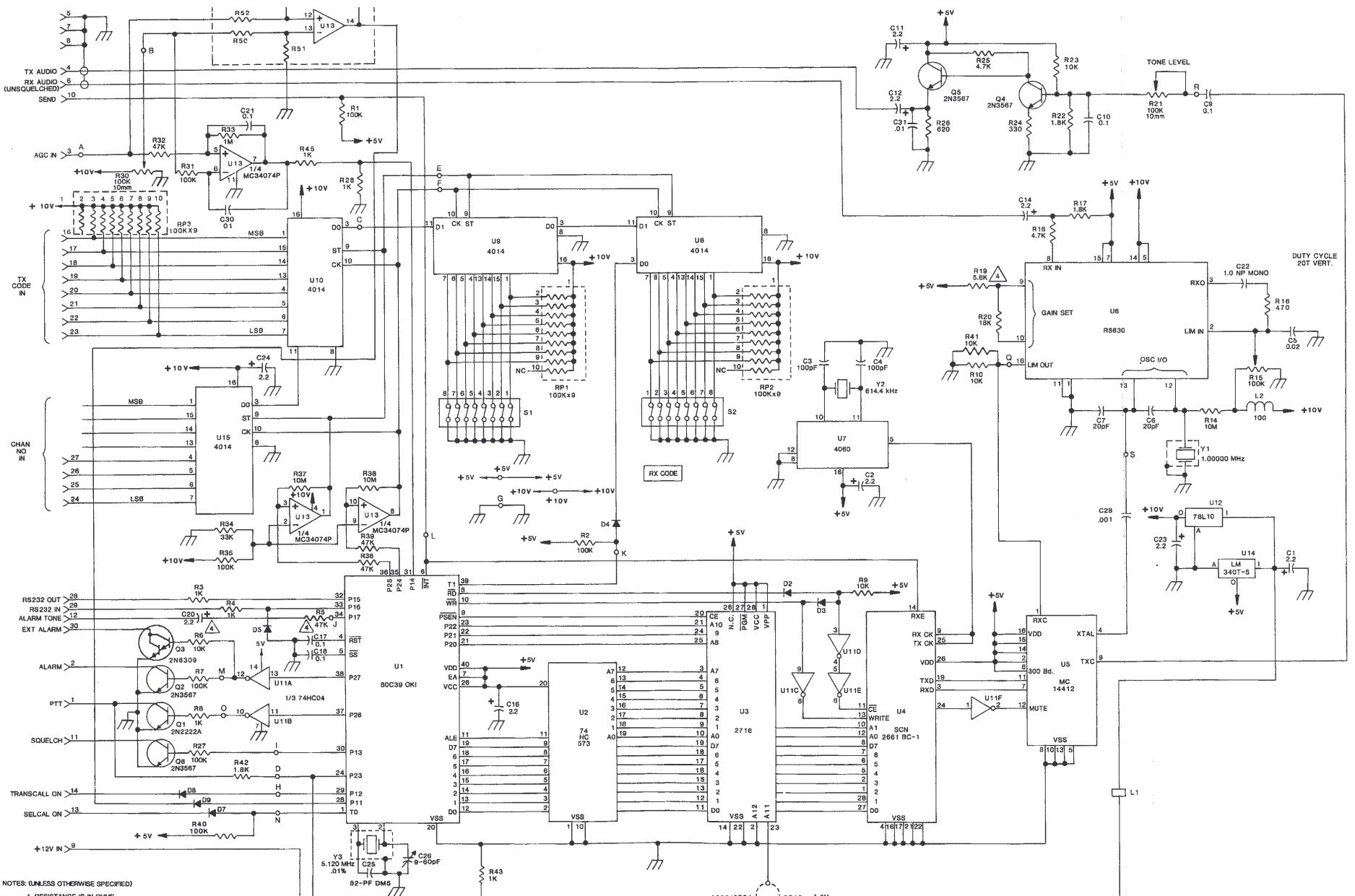


FIGURE 12.2-2.
Component Locations, Selcall and Transcall Option.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTANCE IS IN OHMS.
2. CAPACITANCE IS IN MICROFARADS.
3. DIODES ARE 1N4150

⚠4 FOR PRC-SELCAL OPTION, REMOVE C20 AND REPLACE WITH JUMPER AND CHANGE R5 TO 100 OHMS, REMOVE R10.

990938

TABLE 12.2-8.
Parts List, Selcall and Transcall Option.

C1, C2	241020	Capacitor, Tantalum 2.2 µF
C3, C4	210101	Capacitor, Disc NPO 100 µF
C5	254203	Capacitor, Mylar 0.02 µF
C6, C7	210200	Capacitor, Disc NPO 20 µF
C8		Not Used.
C9	275104	Capacitor, Monolithic 50 V 0.1 µF
C11, C12	241020	Capacitor, Tantalum 2.2 µF
C13		Not Used.
C14	241020	Capacitor, Tantalum 2.2 µF
C15		Not Used.
C16	241020	Capacitor, Tantalum 2.2 µF
C17, C18	275104	Capacitor, Monolithic 50 V 0.1 µF
C19		Not Used.
C20	241020	Capacitor, Tantalum 2.2 µF
C21	275104	Capacitor, Monolithic 50 V 0.1 µF
C22	275105	Capacitor, Monolithic 100 V 1 µF
C23, C24	241020	Capacitor, Tantalum 2.2 µF
C25	221820	Capacitor, Mica DM5 82 pF
C26	261600	Capacitor, Trimmer 9-60 pF
C27		Not Used.
C28	210102	Capacitor, Disc 25 V 0.001 µF
C29		Not Used.
C30,C31	214103	Capacitor, Monolithic 50 V 0.01 µF
D1		Not Used.
D2-D5	320002	Diode, 1N4148
D6		Not Used.
D7-D9	320002	Diode, 1N4148
D10		Not Used.
L1	490302	Bead, Ferrite
L2	430040	Inductor, 100 µH
Q1	310057	Transistor, NPN PN2222A
Q2	310003	Transistor, NPN 2N3567
Q3	310103	Transistor, 2N6039
Q4-Q6	310057	Transistor, NPN PN2222A
R1	113104	Resistor, Film 1/8W 5% 100 kΩ
R2	113103	Resistor, Film 1/8W 5% 10 kΩ
R3, R4	113102	Resistor, Film 1/8W 5% 1 kΩ
R5	113473	Resistor, Film 1/8W 5% 47 kΩ
R6	113103	Resistor, Film 1/8W 5% 10 kΩ
R7	113104	Resistor, Film 1/8W 5% 100 kΩ
R8	113102	Resistor, Film 1/8W 5% 10 kΩ
R9,R10	113103	Resistor, Film 1/8W 5% 10 kΩ
R11-R13		Not Used.
R14	113106	Resistor, Film 1/8W 5% 10 MΩ
R15	170210	Resistor, Trimmer 25T 100 kΩ
R16	113471	Resistor, Film 1/8W 5% 470 Ω
R17	113182	Resistor, Film 1/8W 5% 1.8 kΩ
R18	113472	Resistor, Film 1/8W 5% 4.7 kΩ
R19	113562	Resistor, Film 1/8W 5% 5.6 kΩ
R20	113183	Resistor, Film 1/8W 5% 18 kΩ
R21	170115	Resistor, Trimmer 100 kΩ

TABLE 12.2-8.
Parts List, Selcall and Transcall Option, Continued.

R22	113182	Resistor, Film 1/8W 5% 1.8 kΩ
R23	113103	Resistor, Film 1/8W 5% 10 kΩ
R24	113331	Resistor, Film 1/8W 5% 330 Ω
R25	113472	Resistor, Film 1/8W 5% 4.7 kΩ
R26	113621	Resistor, Film 1/8W 5% 620 Ω
R27	113104	Resistor, Film 1/8W 5% 100 kΩ
R28	113102	Resistor, Film 1/8W 5% 1 kΩ
R29		Not Used.
R30	170115	Resistor, Trimmer 100 kΩ
R31	113104	Resistor, Film 1/8W 5% 100 kΩ
R32	113473	Resistor, Film 1/8W 5% 47 kΩ
R33	113106	Resistor, Film 1/8W 5% 10 MΩ
R34	113333	Resistor, Film 1/8W 5% 33 kΩ
R35	113104	Resistor, Film 1/8W 5% 100 kΩ
R36	113473	Resistor, Film 1/8W 5% 47 kΩ
R37, R38	113106	Resistor, Film 1/8W 5% 10 MΩ
R39	113473	Resistor, Film 1/8W 5% 47 kΩ
R40	113104	Resistor, Film 1/8W 5% 100 kΩ
R41	113103	Resistor, Film 1/8W 5% 10 kΩ
R42	113182	Resistor, Film 1/8 W 5% 1.8 kΩ
R43	113102	Resistor, Film 1/8 W 5% 1 kΩ
R44		Not Used.
R45	113102	Resistor, Film 1/8W 5% 1 kΩ
RP1-RP3	182002	Resistor Pak 100 Ω
S1	530010	Switch, Scan Limit/Options
S2	530010	Switch, RX Code
U1	330142	IC, 80C39
U2	330141	IC, 74HCT573
U3	330102	IC, UPD2716-6
U4	330167	IC, SCN2661BC1N28
U5	330180	IC, MC 14412VP
U6	330215	IC, RM5630AP
U7	330037	IC, CD 4060 BE
U8-U10	330181	IC, MC 14014BCP
U11	330196	IC, 74HCO4
U12	330300	IC, UA78L10CLP
U13	330220	IC, MC34074P
U14	330076	IC, LM340
U15	330181	IC, MC14014BCP
Y1	360028	Crystal, 1.000 MHz Microprocessor
Y2	363001	Resonator, Ceramic 614.4 kHz
Y3	360018	Crystal, 5,120.000 kHz

12.3 WIDEBAND FILTER OPTION

12.3.1 GENERAL

This option involves using 1.650-MHz crystal filters having a bandwidth of 300-3100 Hz instead of the standard 300-2700 Hz. These are designed for special applications such as high-speed data requiring greater bandwidth and tighter control of group delay.

12.3.2 INSTALLATION

Both USB and LSB wideband filters can be obtained. They replace the standard crystal filters in the transceiver's M2 module. Part number differences between the standard filter M2 and the optional wideband filter M2 are shown in Table 12.3-1.

TABLE 12.3-1.
Filter Part Number Differences.

	Standard Filter	WB Filter	Quantity/ Designator
USB	361002 361004	361052 361054	(1)-Y4 (2)-Y2,Y6
LSB	361006 361008	361056 361058	(2)-Y7,Y11 (1)-Y9

12.4 ARQ OPTION

12.4.1 INTRODUCTION

The ARQ option is installed in transceivers used for ARQ (Sitor) operation. The purpose of this option is to provide electronic switching of the +12 Vdc to the transmit and receive circuitry. When this option is used, the relay provides only the sense voltage and the contacts do not carry significant currents. This means that the relay will normally operate for its rated mechanical life of 20 x 106 cycles without appreciable contact wear.

12.4.2 INSTALLATION

In the TW100F, the ARQ option is contained on PCB 735149 and is installed between the M8 and the M10 modules. The top traces between the pins R+ and R+ sense and T+ and T+ sense on the left side of M7 (view from the front of transceiver) are cut. The module is connected as shown in Figure 12.4-1.

12.4.3 CIRCUIT DESCRIPTION

Q1 is an electronic switch in the T+ line to the transmitter exciter. Q1 is controlled by Q15 on M7. When the T/R relay closes, +12 V is applied to the base of Q15 which conducts pulling the R+ sense line low. This, in turn, forward biases the PNP transistor Q1, thus switching the T+ voltage on.

Q2 is an electronic switch in the R+ line to the receiver. Q2 is controlled by Q3 which is connected to the R+ sense line. When the T/R relay is open (in the receive mode), R+ sense is applied to the base of Q3, pulling the base of Q2 low. As Q2 is a PNP transistor, this applies forward bias through R1, causing Q2 to conduct, turning the R+ on.

Q4 is a clamp on the R+ line and is used to prevent any slow decay after switching. The base of Q4 is connected to T+ and causes Q4 to conduct and clamp the R+ line.

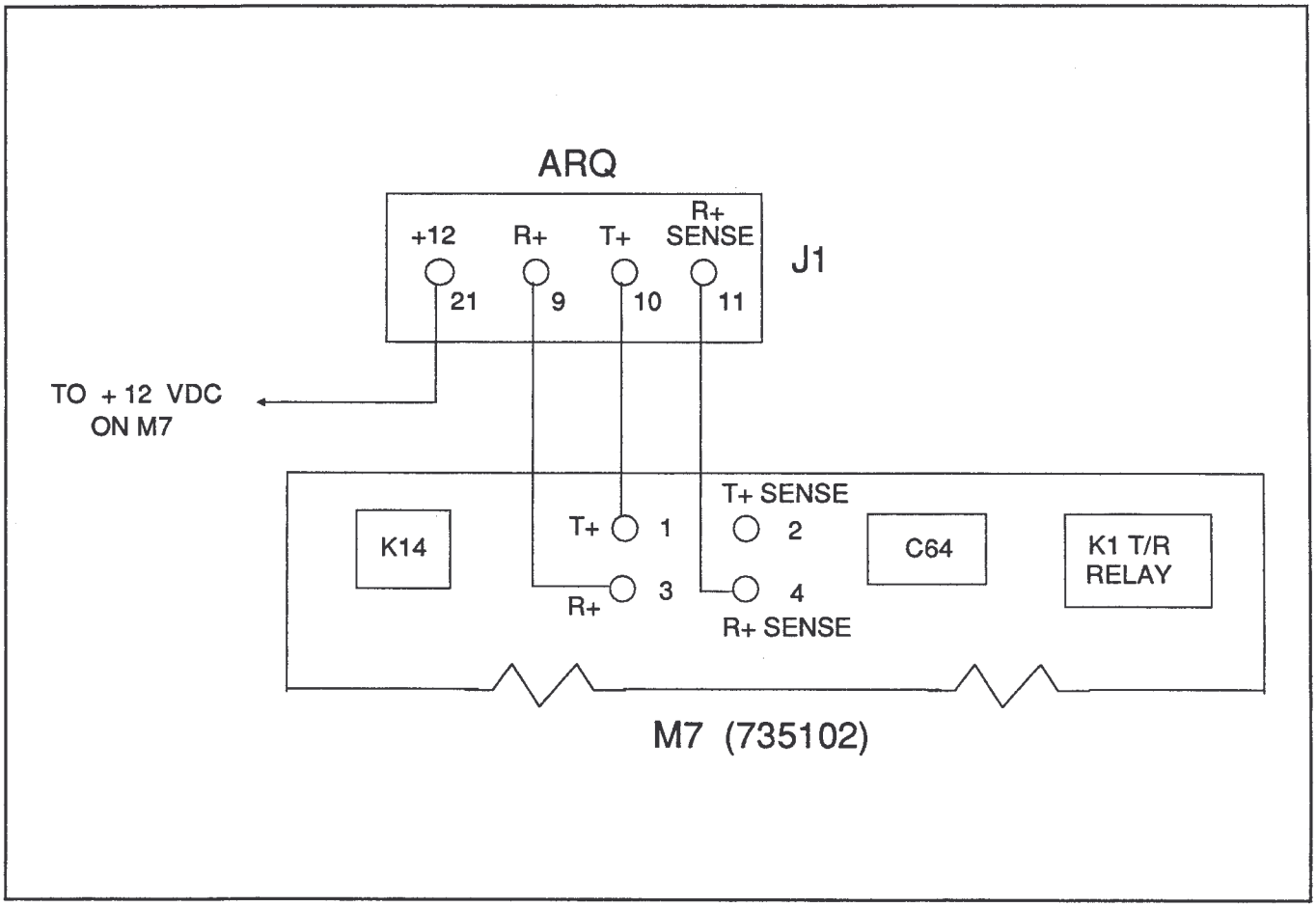


FIGURE 12.4-1.
ARQ Connections.

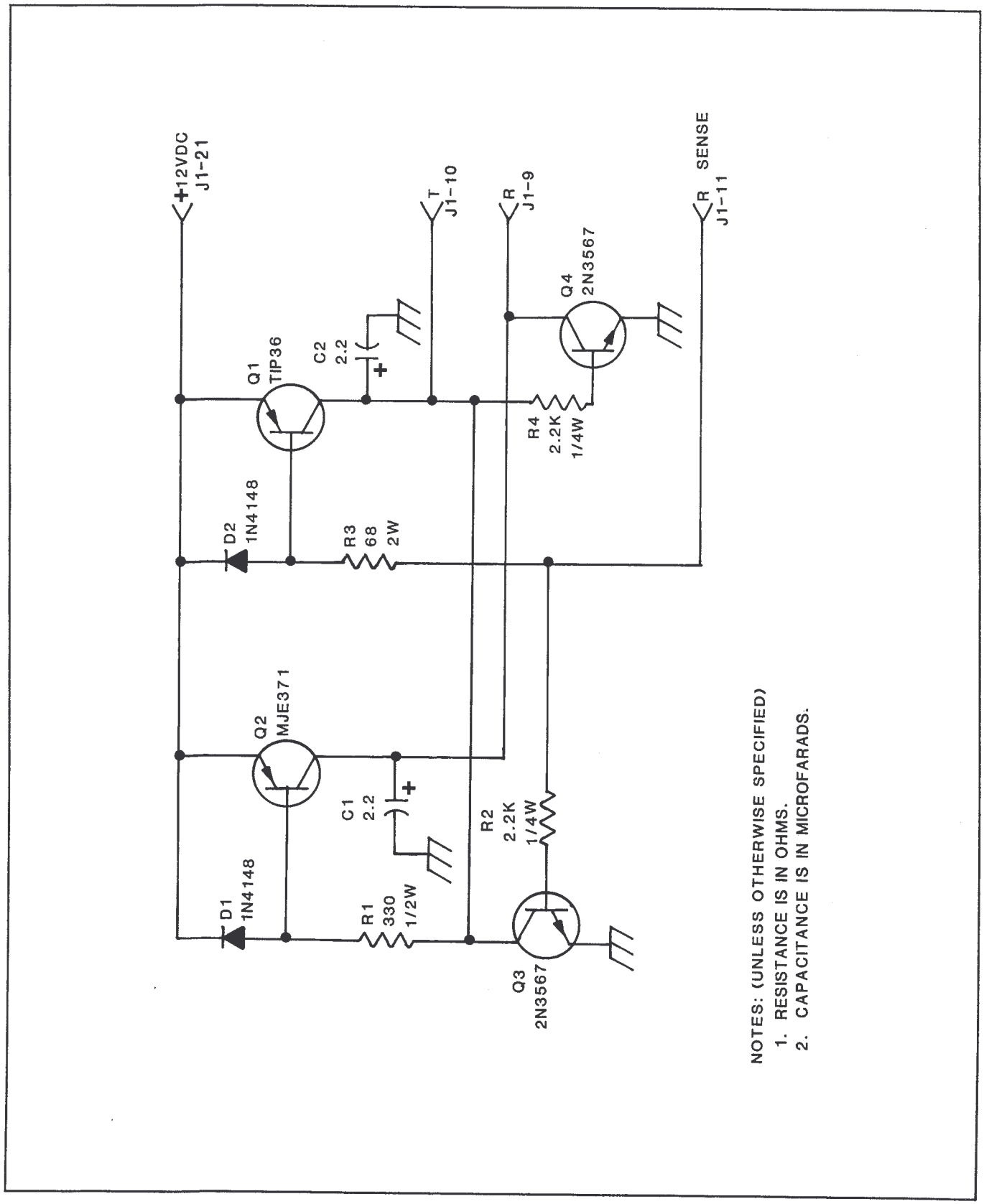


FIGURE 12.4-2.
Schematic Diagram, ARQ Option.

TABLE 12.4-1.
Parts List, ARQ Option.

C1,C2	241020	Capacitor, Tantalum 2.2 μF
D1,D2	320002	Diode, 1N4148
Q1	310068	Transistor, TIP36A
Q2	310035	Transistor, PNP MJE371
Q3,Q4	310003	Transistor, NPN 2N3567
R1	134331	Resistor, Comp 1/2 W 5% 330 Ω
R2	124222	Resistor, Film 1/4 W 5% 2.2 kΩ
R3	154680	Resistor, Film 2 W 5% 68 Ω
R4	124222	Resistor, Film 1/4 W 5% 2.2 kΩ

APPENDIX A

A-1 GENERAL

A basic knowledge of the techniques used in the synthesizer design is necessary for both understanding and troubleshooting these circuits. The transceiver has two completely independent synthesizers, one providing the 76.6 to 104.99-MHz signal for the First Local oscillator and the other providing the 73.3401 to 73.350-MHz signal for the Second Local oscillator. The heart of both synthesizers is a phase-locked loop; a brief analysis of phase-locked loops is given in this section. Another important concept used in the design of the synthesizer is dual-modulus prescaling. The knowledge of this concept is important not only in the understanding of the synthesizer design, but also in the programming of the transceiver radio frequencies.

This section includes a block diagram of the overall synthesizer. The description of the block diagram is shown in relation to the techniques of the phase-locked loop and dual-modulus prescaling in order to give a better understanding of the operation of the synthesizer. An example illustrating the frequency programming of each synthesizer loop demonstrates the mathematical algorithms used and their relationship to the overall frequency conversion scheme.

Also shown in this section is a description of the frequency scheme used in the transceiver. Numerical examples are provided to clearly illustrate this approach. The overall frequency stability of the transceiver is also discussed, and an equation is developed which shows how the stability criterion is established.

A-2 BLOCK DIAGRAM DESCRIPTION

A block diagram of the synthesizer is shown in Figure A-1. It is composed of two completely independent single-loop digital synthesizers. The 10-kHz Loop uses a VCO phase-locked to a 10-kHz reference frequency. This choice of reference frequency enables using a loop bandwidth high enough for good stability and switching speed, and also low enough for good reference spurious suppression. The 10-kHz Loop is a single-loop synthesizer using no mixing or multiplication, and as such has excellent spectral purity. The 100-Hz Loop uses a VCXO phase-locked to a 100-Hz reference frequency. The very stable crystal oscillator is "pulled" over a 10-kHz range using the 100-Hz PLL. Because of the inherent stability and purity of crystal oscillators, the 100-Hz Loop provides an exceptionally good I.O. signal for the Second Mixers.

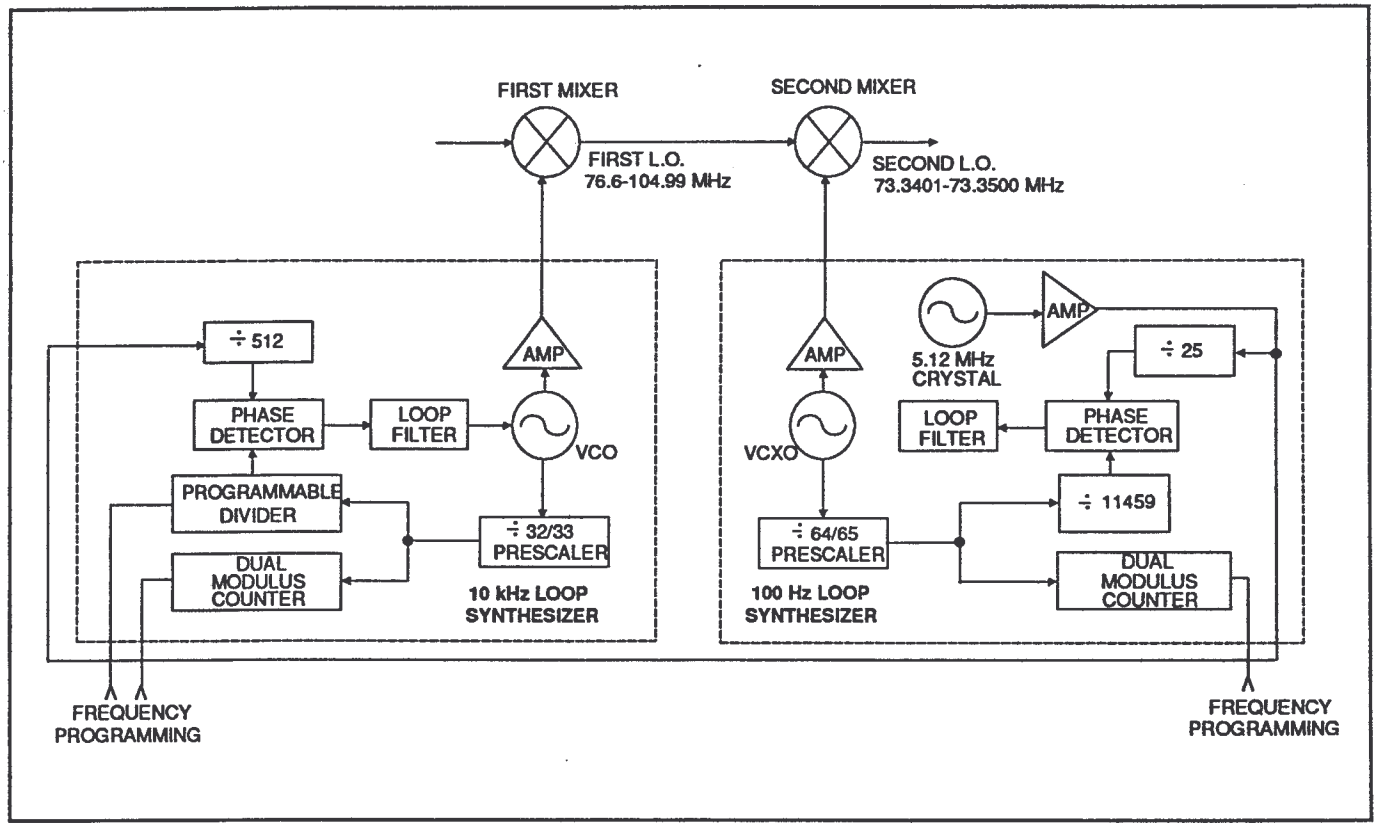


FIGURE A-1.
Synthesizer Block Diagram.

A-3 PHASE-LOCKED LOOPS

The heart of each synthesizer is the phase-locked loop (PLL), a simplified diagram of which is depicted in Figure A-2. Referring to this diagram, it is seen that a PLL consists of the following basic elements:

1. A Voltage Controlled Oscillator (VCO).
2. A Phase Detector.
3. A Divider; either fixed (+M) or Variable (+N).
4. A Loop Filter.

The purpose of a PLL is to provide a VCO, which operating alone might be unstable, with the stability and accuracy of a single, highly stable reference frequency. The inputs to the phase detector are a reference frequency (generally a very stable temperature-controlled crystal oscillator), and the VCO output frequency divided by the integers N x M. The phase detector dc output controls the VCO frequency, and under proper PLL conditions, will change the VCO frequency (divided by M x N) to equal the reference frequency. The +M is generally a fixed divider called a prescaler, whose purpose is to reduce a high VCO frequency to a lower level that can be handled by standard programmable logic system.

The +N can be either a fixed or a variable divider. When N is variable, it can be programmed externally to change the VCO frequency in discrete steps. The phase detector will electronically tune the VCO each time N is changed to bring the output of the divider to the same frequency and phase as that of the reference. The loop is locked when $F_{out} = NMF_{ref}$.

Once the loop is locked, operation proceeds as follows: If the output frequency increases, the frequency out of the divider will exceed F_{ref} and the phase detector will react by trying to drive the VCO frequency lower. The tuning voltage to the VCO will decrease as a result and the output frequency will decrease, which counters the initial frequency increase. The loop filter is present to suppress undesired components produced in the phase detector so they don't cause unacceptable FM on the VCO. The loop filter also has an important effect on other types of noise, on acquisition of lock, loop response time, and stability.

In a PLL synthesizer, the error signal driving the VCO changes value only once each reference period; the loop bandwidth, which determines response speed, is set to be approximately one-tenth the reference frequency. This is necessary for stability and for suppression of the reference frequency sidebands. The higher the reference frequency, the faster the loop response time; but the reference frequency also determines the minimum synthesizer channel spacing. For example, if the reference frequency is 10 kHz, the MINIMUM channel spacing is 10 kHz. If the fixed divider M in Figure A-2 is greater than one, the F_{out} can only be changed in steps of MF_{ref}. If M is made equal to one, then the channel spacing depends only on F_{ref}.

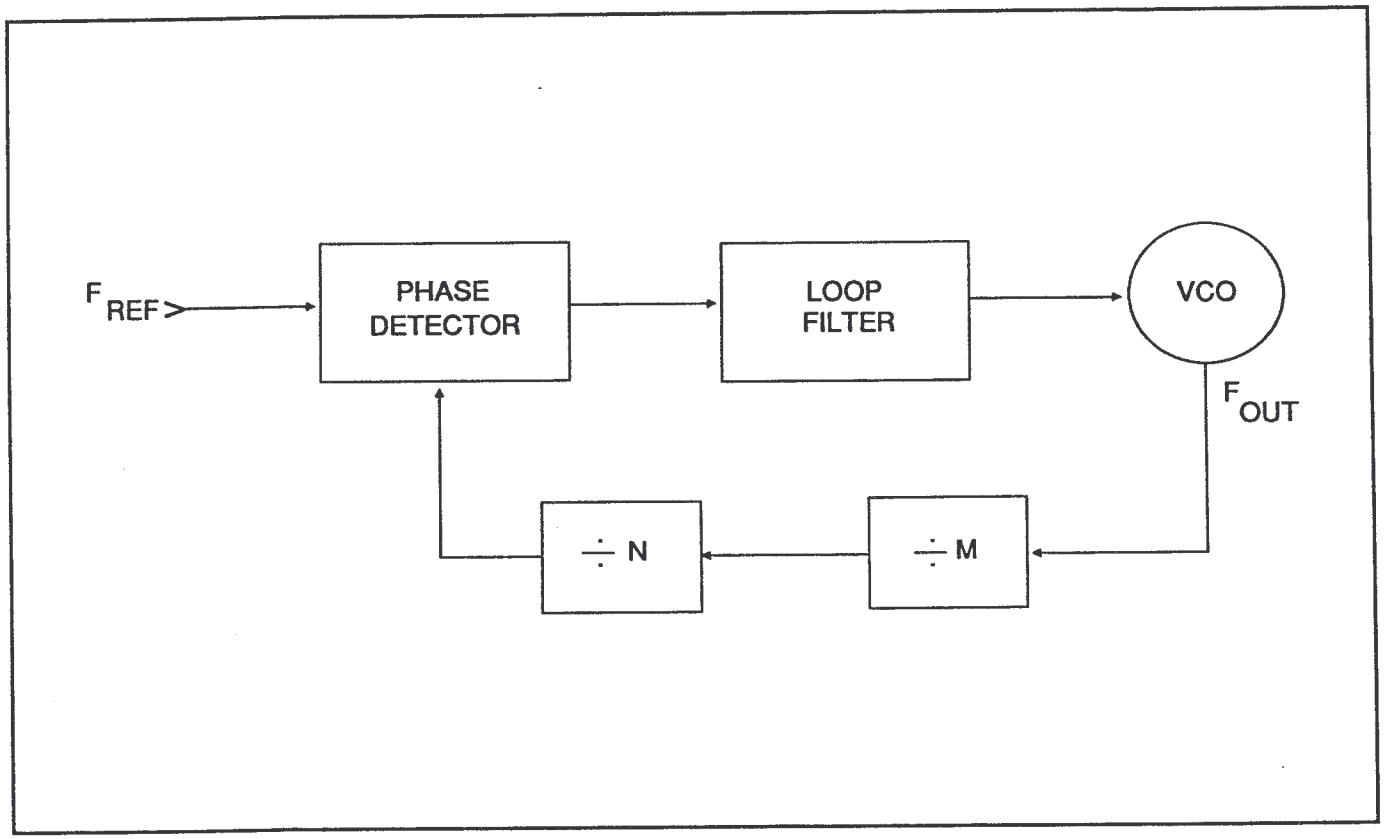


FIGURE A-2.
Phase-Locked Loop.

In our case, the ultimate channel spacing is 100 Hz. But to make a single-loop synthesizer with a 100-Hz reference covering a 28-MHz range would place severe restrictions on loop response time as well as VCO stability. Thus, the transceiver uses two synthesizers: the 10-kHz Loop covering 76.6-104.99 MHz with 10-kHz channel spacing which provides a loop BW high enough for good response time and stability, and a 100-Hz Loop covering 10 kHz in 100-Hz steps using a high-stability crystal oscillator.

A-4 DUAL-MODULUS PRESCALING

CMOS dividers provide not only the lowest power approach, but also the best approach for spectral purity because of their switching response. However, CMOS dividers are restricted in operating speed to below 10 MHz for reliable operation.

With the 10-kHz Loop operating at 76.6-104.99 MHz, and the 100-Hz Loop at 73 MHz, it is clear that some form of prescaling (or +M) is required to reduce the VCO frequency to a level that can be handled by standard CMOS programmable dividers, and still the channel spacing needed for 10-MHz and 100-Hz loops.

The synthesizers solve this problem by using a technique known as dual-modulus prescaling. This approach allows low-frequency CMOS programmable counters to be used as high-frequency programmable counters with speeds of several hundred MHz. This is possible without the sacrifice in channel spacing and performance that would otherwise result if a fixed divider was used for the prescaler (-M). Prescalers are used whose division ratio can be switched between two values to allow effective division at the high prescaler input frequency (VCO output), with the actual programmable dividers operating at the lower output frequency of the prescaler.

Figure A-3 illustrates how a dual-modulus divider system operates. The VCO drives the dual-modulus prescaler (which can divide by P and P+1), which in turn drives two programmable counters in parallel. These two counters are programmed to "A" and "N". The prescaler and the A-counter are connected in such a way that in a complete count cycle, the prescaler divides by P+1 until the A-counter reaches zero and then reverts to a division ratio of P. Both the A-counter and the N-counter start counting at the same time. Therefore, the prescaler divides by P+1 for "A" counts and by P for "N-A" counts. For example, the programmed divide ratio N_T is:

$N_T = (N-A)\,P + A(P+1)$
or
$N_T = NP + A$

Therefore, the overall divider system divides by P+1 for as long a count as the A-counter is programmed (A counts), and then divides by P for the remainder of the cycle (N-A counts). The only restriction on the scheme is that the total count cycle (N) be greater than A.

For example, the 10-kHz Loop Synthesizer (as shown in Figure A-1) uses a +32/33 prescaler (an MC12015 rated at

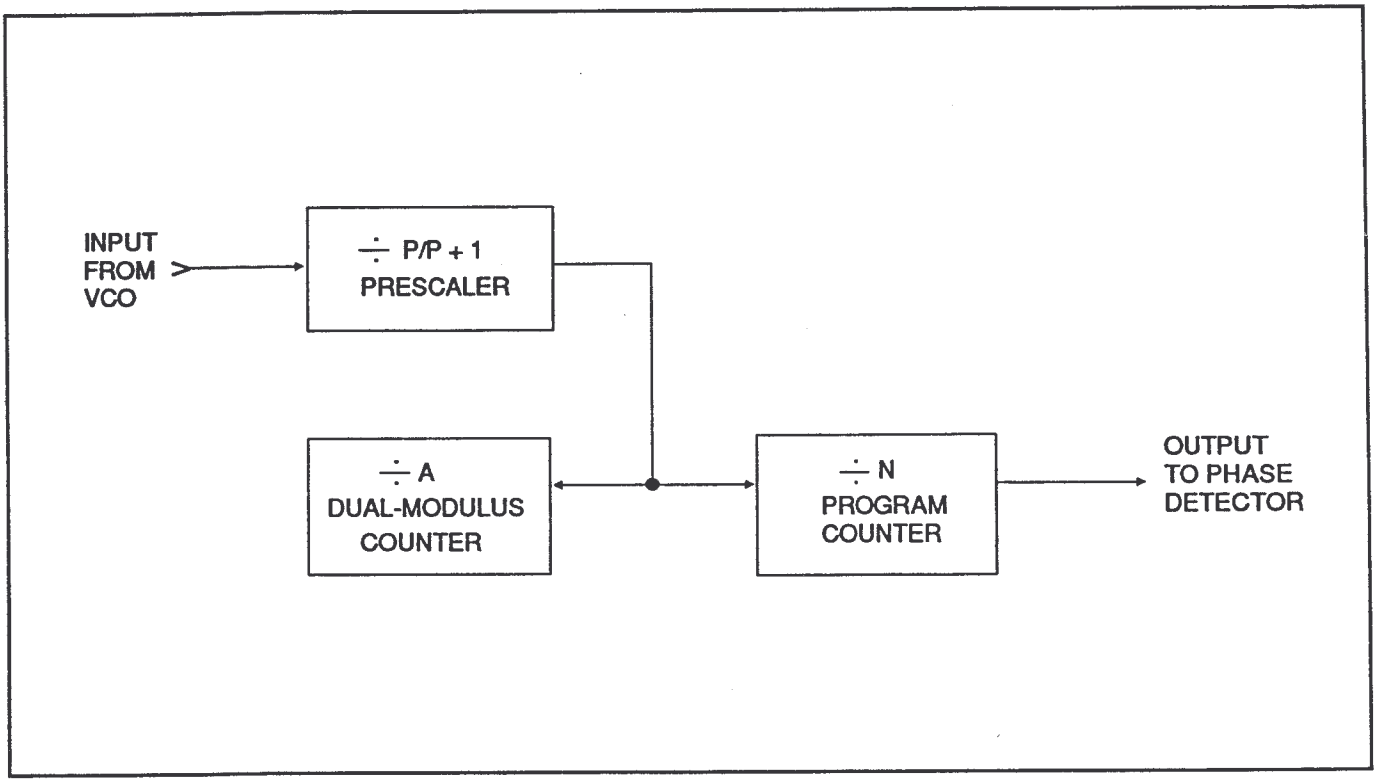


FIGURE A-3.
Dual-Modulus Prescaler.

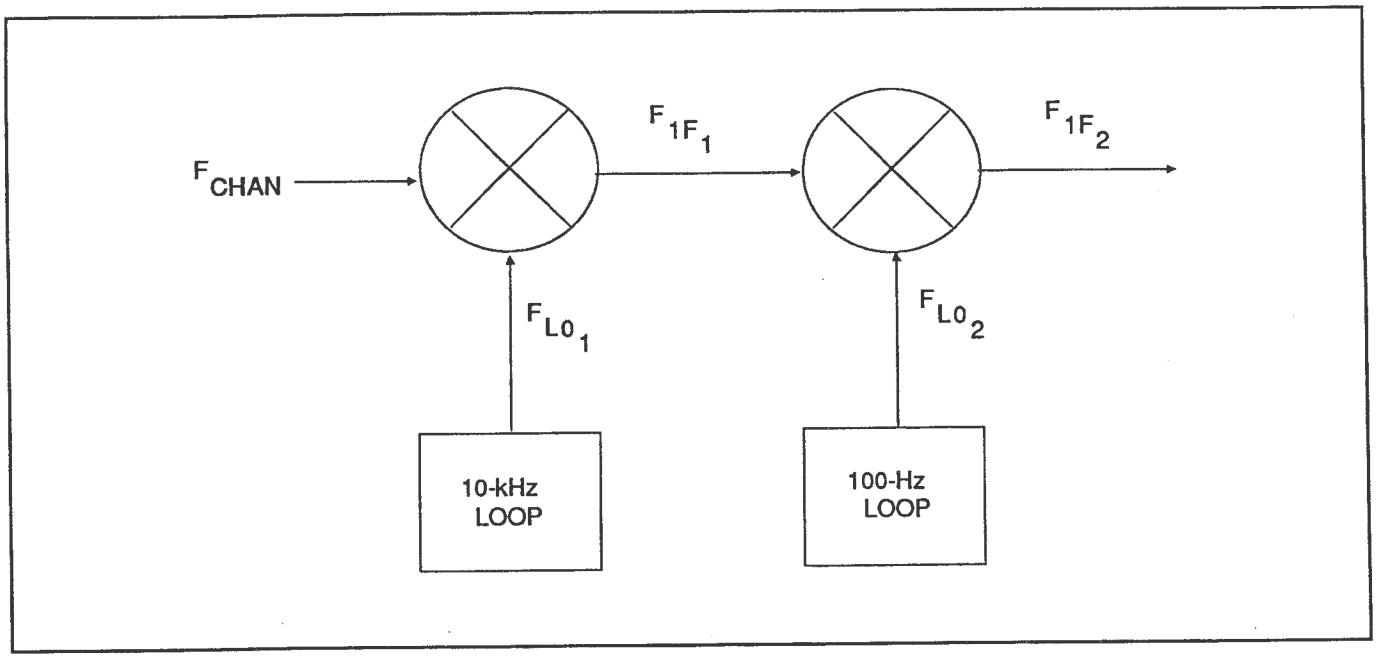


FIGURE A-4.
Frequency Scheme.

200 MHz). The highest VCO frequency is 105 MHz, which when divided by 32 equals 5—well below the 30-MHz MC145152 CMOS counting speed. If the selected channel frequency is 25 MHz, then the VCO frequency is 25 + 75 = 100 MHz. The total divide ratio is: $N_T = F_{out}$ $F_{ref} = NP + A$; or N_T 100 x $10^6/10^4 = NP + A$. Therefore, the total division ratio is 10,000 and with P = 32, the equation division ratio is 10,000 and with P = 32, the equation is:

10,000 = 32N + A,
or
N = 312, and A = 16

Then 312 is the number programmed into the N-counter and 16 is the number programmed into the A-counter. The +32/33 prescaler then divides by 33 for 10 counts and 32 for 296 counts to account for the overall division ratio of 10,000.

33 x 16 = 528
32 x 296 = 9472
∴528 + 9472 = 10,000

The 100-Hz Loop Synthesizer (Figure A-1) uses a +64/65 prescaler with a frequency limit of 200 MHz. The VCXO frequency is 73.3401-73.3500 MHz. Therefore, the output of the prescaler into the programmable divider is approximately 1 MHz. Since this loop has only 100 discrete frequencies (73.3401-73.350 MHz in 100-Hz steps) all the programming can be done in the dual-modulus counter (set for count from 1-100), while the +N programmable counter has a fixed division ratio of 11459. The total 100-Hz Loop divide ratio is:

$N_T = 64N+A$, or $N_T = 64 \times 11459 + A$

which is:

$N_T = 733376 + A$

This means that the loop will divide by 65 for "A" counts, and then divide by 64 for (11459-A) counts.

A-5 FREQUENCY PROGRAMMING EXAMPLE

To illustrate the concept of dual-modulus prescaling used in the synthesizer, the following example is presented:

EXAMPLE:

Let the selected channel frequency be 9,124,200 Hz. The 10-kHz Loop programming then goes as follows:

1. The first L.O. output frequency is:
09.12 + 75.00 = 84.12 MHz

2. Using the formula developed earlier for the 10-kHz Loop:
$N_T = F_{out}/F_{ref}$ = 84,120,000/10,000
= 8412
3. Therefore, the total division ratio for the 10-kHz Loop is N_T = 8412.

4. Since N_T = 32N + A, where "N" is the number programmed into the variable programmable counter, and "A" is the number programmed into the dual modulus counter then,

8142 = 32N + A
∴N = 8142/32 = 254

Then, A = 8142 - 254 x 32 = 14

5. The total 10-kHz Loop counter cycle is then 254, with the loop dividing by 33 for 14 counts and by 32 for 254 - 14 = 240 counts. Thus, N_T = (33 x 14 = 462) + (240 x 32 = 7680) = 8142.

6. With the 10-kHz Loop at 84.12 MHz and the channel frequency at 9.1242 MHz, the First IF is 74.9958 MHz (or 4.2 kHz below the center of the 75-MHz IF filter passband). The Second L.O. is then:

Second L.O. = 74.9958 - 1.65 = 73.3458 MHz

7. 100-Hz Loop programming is done by first looking at the 1-kHz and 100-Hz digits of the channel frequency (in this case, 9.1242 MHz).

a. Let these two digits equal EF. Then A = 124 - EF.
b. In this case, the two digits are 42.
Therefore, A = 124 - 42
= 82.

8. The dual-modulus frequency formula for the 100-Hz Loop is then applied:

N_T = 11459 x 64 + A

N_T = 733376 + 82
= 733458

9. The output frequency is then $F_{LO} = F_{ref}$ x N, or FLO = 733,458 x 100 Hz = 73.3458 MHz, which corresponds with the frequency determined in part 6.

A-6 FREQUENCY CONVERSION SCHEME

This simplified diagram in Figure A-4 illustrates the overall frequency scheme.

Frequencies shown are as follows:

F_{chan} = RF channel frequency of the radio; 1.600-29.9999 MHz, selectable in 100-Hz increments resulting in 284,000 available channels.

F_{LO1} = Output of the 10-kHz Loop, a phase-locked loop (PLL) synthesizer generating a 76.60 to 104.99-MHz output in 10-kHz increments.

F_{IF1} = First IF; varies between 75.000 and 74.9901 MHz depending on the chosen channel frequency.

F_{LO2} = Output of the 100-Hz Loop, a PLL synthesizer operating from 73.3401-73.350 MHz in the 100-Hz increments.

F_{IF2} = Second IF; fixed at 1.65 MHz.

A-7 EXAMPLES OF OSCILLATOR FREQUENCIES

Table A-1 shows the oscillator injection frequencies for a few sample channel RF frequencies. Note that the first IF frequency is not fixed at 75.00 MHz but varies over a 10-kHz range depending on the selected channel frequency. This is accomplished as follows:
$f_{LO1} = f_{chan}$ + 75.00 MHz*

1. The first IF is always:
$F_{IF1} = F_{LO1} - f_{chan}$

2. The second IF is always fixed at 1.65 MHz. Therefore, the second L.O. is:
$F_{LO2} = F_{IF2}$ - 1.650 MHz

***NOTE**

Only the first four digits of the channel frequency are used in determining FLO1.

EXAMPLE:
f_{chan} = 2,000,000 Hz, and
f_{chan} = 2,005,900 Hz

Both result in F_{LO1} = 2.00 + 75.00 = 77.00 MHz (remember that the first digit is always the 10-MHz digit; therefore, the first four digits of 2,000,000 Hz are 02.00).

A-8 FREQUENCY STABILITY

Since both local oscillators are locked to a single reference frequency, the frequency errors in the two oscillators due to a change in reference frequency will tend to cancel each other. Therefore, the overall radio frequency error due to a shift in the reference is proportional to the difference in the two L.O. frequencies. The following is the equation for overall system frequency shift due to a shift in the reference frequency:

$$f_{system} = \frac{F_{LO1} - F_{LO2}}{F_{ref}} (f_{ref})$$

where:
f_{system} = System Frequency Shift
F_{LO1} = first L.O.
F_{LO2} = second L.O.
f_{ref} = 5.120 MHz
f_{ref} = drift in F_{ref} from 5.120 MHz

The transceiver's reference oscillator uses a 5.120-MHz crystal oscillator. Stabilities in the order of ±5 ppm can be achieved in this fashion. This translates into a 25.6-Hz drift in reference frequency over the specified -30°C to +55°C temperature range. The total frequency drift of the radio is then:

At 2 MHz:
$f_{system} = \frac{77 - 73.35}{5.12}$ x 25.6 = 18.25 Hz

At 30 MHz:
$f_{system} = \frac{105 - 73.35}{5.12}$ x 25.6 = 158.25 Hz

TABLE A-1.
Example Frequencies.

F_{chan}	F_{LO1}	F_{IF1}	F_{LO2}	F_{IF2}
2.0000	77.0000	75.0000	73.3500	1.6500
2.0001	77.0000	74.9999	73.3499	1.6500
2.0099	77.0000	75.9901	73.3401	1.6500
2.0100	77.0100	75.0000	73.3500	1.6500
3.0000	78.0000	75.0000	73.3500	1.6500
29.9999	104.9900	74.9901	73.3401	1.6500

NOTE

As F_{chan} goes through 10-kHz (e.g. from 2.000-2.0099), F_{LO1} remains the same frequency (77.0000 MHz), and F_{LO2} makes one hundred 100-Hz steps (from 73.3500 to 73.3401).